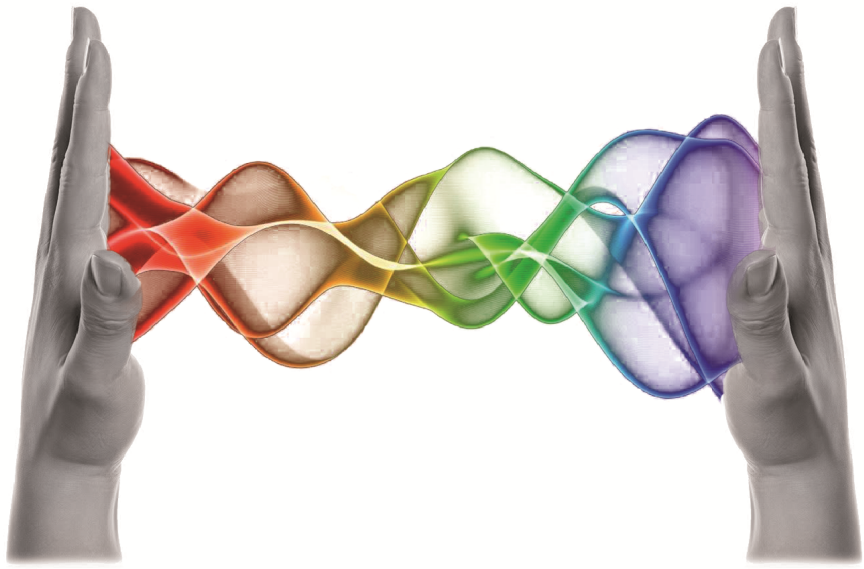
Micromachined Parallel Plate Structures For Casimir Force Measurement And Optical Modulation



Mubassira Banu Syed Nawazuddin

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Cover Design by: R. Kottumakulal Jaganatharaja
Front cover: Two hands acting as parallel plate boundary and the waves as the quantum vacuum fluctuations that fits within the boundary. Back cover: Clockwise from left (top): SEM image of bonded parallel plate structures for Casimir force measurement; Red light propagating through the TripleX waveguide; and the SEM image showing the top view of waveguide with anti-stiction bumps.

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Micromachined Parallel Plate Structures for Casimir Force Measurement and Optical Modulation

DISSERTATION

to obtain
the degree of doctor at the University of Twente,
on the authority of the rector magnificus,
prof. dr. H. Brinksma,
on account of the decision of the graduation committee,
to be publicly defended
on Friday, 22 November 2013 at 16:45

by

Mubassira Banu Syed Nawazuddin

born on 5 December 1982,
in Chidambaram, India

This dissertation is approved by

Prof. Dr. M. C. Elwenspoek	University of Twente (Promotor)
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Contents

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Sometimes our light goes out, but is blown again into instant flame by an encounter with another human being. Each of us owes the deepest thanks to those who have rekindled this inner light - Albert Schweitzer.

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Mubassira
October 2013,
London, United Kingdom.

Abstract

In microelectromechanical systems (MEMS), parallel plate structures with sub-micron separation have been of much use in various types of sensors and actuators. In this thesis such parallel plate structures are employed for two applications viz. the Casimir force measurement and to develop a mechano-optical modulator. Both research studies are focussed on realising parallel plate structures with a separation distance in the order of 1 μm or less.

The Casimir force in its original form is formulated between two uncharged parallel metallic plates in vacuum, at zero temperature. Previously, many research groups have successfully attempted quantifying the Casimir force with different measurement configurations viz. sphere-plate, crossed cylinders and plate-plate. The plate-plate configuration gives the largest interaction area, but keeping the plates exactly parallel at sub-micrometer separation is a very demanding task. In this thesis, a methodology to measure the Casimir force using parallel plate structures is described, in which MEMS technology is used to improve the parallelism at sub-micrometer separations. The fabrication of these parallel plate structures is described and a dynamic measurement methodology to determine Casimir force using a scanning laser vibrometer is developed. The scanning laser vibrometer allows monitoring the movement of both plates; one actuated and one suspended by flexures, where the movement of the latter is defined by the forces acting between the plates. Different measurement techniques are developed which allows the measurement of the Casimir force between parallel plates in terms of plate vibration amplitude.

To realise the parallel plates separated at $\sim$1 μm distance, two fabrication processes based on two different substrates, namely <111>-oriented silicon and silicon-on-insulator (SOI) wafers have been developed. The main goal of the fabrication process based on the <111>-oriented substrate is to obtain ultra-smooth surfaces on the plate surface area,

which are defined by the <111> crystal planes. The resulted surface roughness is in the order of ∼3 nm. Further, fusion bonding was used to bond the wafers containing the two plates together. This ultimately results in the final device consisting entirely of mono-crystalline silicon and is, therefore, relatively insensitive to temperature variations. The fabrication process based on SOI substrates was mainly developed to result in good fabrication yield, sufficient surface smoothness and a strong bond between the top and bottom plates. Both fabrication processes resulted in parallel plate structures, however, only devices based on the SOI process were suitable for performing measurements. So far, no successful Casimir force measurements have been performed, however the obtained results do indicate that the measurement strategy is feasible and the research along this route should be continued.

The second part of the thesis deals with the design and realisation of an IONM (Integrated Optical Nano-Mechanical) based mechano-optical modulator. The mechanical structure and the optical waveguide are realized on separate chips and then assembled together resulting hybrid integration. A multi-layer waveguide named TripleX waveguide developed by Lionix B.V. is used as an optical waveguide. The mechanical element is made of a light-weight, rigid silicon-nitride suspended plate structure with a thin layer of gold on top for optical modulation. The hybrid integration is made possible by using a self-alignment technique which results in a misalignment error of at most 2 μm. A bi-directional electrostatic actuation is applied between the mechanical element and the optical waveguide to maximize the switching speed.

The major part of this research study is focussed on the design and optimisation of the light-weight mechanical element that can be integrated with any optical waveguide. One important characteristic of the mechanical structure is the inclusion of ridges underneath the beam. These ridges are included to keep the beam flat and also to avoid stiction of the mechanical beam to the substrate when operated towards pull-in. The integrated mechano-optical modulator device is characterised for both the electrical and optical measurements. The Capacitance-Voltage (CV) measurements successfully demonstrated the bi-directional electrostatic actuation of the device. This measurement also confirmed the movement of the mechanical beam in close vicinity of the waveguide core. From these results, it is shown that the mechanical structure can be actuated towards and away from the waveguide, demonstrating successful self-aligned assembly. However, a redesign will be necessary with an improved waveguide design to be able to actually observe mechano-optical modulation.

Samenvatting

In micro-elektromechanische systemen (MEMS) worden parallelle-plaat-structuren met zeer geringe onderlinge afstand veelvuldig gebruikt voor de realisatie van sensoren en actuatoren. In dit proefschrift worden dergelijke structuren onderzocht voor twee verschillende applicaties: het meten van Casimir-kracht en een mechanisch-optische modulator. Beide onderzoeken zijn gericht op het realiseren van parallelle-plaat-structuren met een onderlinge afstand van een micrometer of minder.

De Casimir-kracht wordt klassiek beschreven als de kracht die twee ongeladen metalen platen in een vacuüm ondervinden, bij het absolute nulpunt. Vele onderzoeksgroepen hebben in het verleden succesvol onderzoek gedaan naar het kwantificeren van Casimir-kracht waarbij gebruik is gemaakt van verschillende meetconfiguraties, te noemen: bol-plaat, kruisende cilinders en plaat-plaat. De plaat-plaat configuratie geeft het grootste interactieoppervlak, maar het parallel houden van de platen bij sub-micrometer afstand is zeer moeilijk uitvoerbaar. In dit proefschrift wordt een methodologie beschreven voor het meten van Casimir-krachten door middel van parallelle-plaat-structuren, waarbij MEMS-technologie wordt gebruikt om de platen afstand zo goed mogelijk parallel te houden bij sub-micrometer afstand. De fabricage van degelijke parallelle-plaat-structuren wordt beschreven, evenals een dynamische meetmethode om de Casimir-kracht tussen deze platen te bepalen. De ontwikkelde methode bestaat uit een vrij opge-hangen plaat die parallel is gepositioneerd ten opzichte van een transleerbare plaat met een onderlinge afstand van een micrometer. De transleerbare plaat wordt vervolgens op en neer bewogen in de richting van de vrij opgehangen plaat en met behulp van een scannende Laser-Doppler vibrometer wordt nauwkeurig naar de beweging van beide platen gekeken. De beweging van de vrij opgehangen plaat hangt af van de onderlinge krachten tussen de platen, waaraan de Casimir-kracht ook een bijdrage kan leveren. Er zijn verscheidende

meetmethodes ontwikkeld om Casimir-kracht te kunnen bepalen waarbij gebruik wordt gemaakt van de vibratieamplitude van de platen.

Om de parallelle-plaat-structuren te realiseren zijn er twee fabricagemethodes ontwikkeld. De eerste methode is gebaseerd op een <111>-georiënteerd silicium substraat om zeer gladde oppervlakken te verkrijgen die gedefinieerd worden door het <111>-kristalvlak. De gemeten oppervlakteruwheid hierbij is rond de drie nanome-ter. Verder is er gebruik gemaakt van fusiebonden om twee delen van de parallelle-plaat-structuur met elkaar te verbinden, waarbij elk deel een plaat bevat. Dit resul-teert in een geheel dat volledig uit monokristallijn silicium bestaat en daarom vrijwel ongevoelig is voor temperatuurvariaties. De tweede fabricage methode is gebaseerd op een *silicon-on-insulator* (SOI) substraat en is voornamelijk ontwikkeld om een robuuster fabricageproces te verkrijgen. Beide fabricage processen hebben geresulteerd in parallelle-plaat-structuren. Echter, alleen de structuren gebaseerd op het tweede pro-ces waren geschikt om metingen mee uit te voeren. Helaas zijn er tot nu toe (nog) geen succesvolle Casimir-kracht metingen uitgevoerd. Echter, de verkregen resultaten tonen de potentie van de meetmethode aan en verder onderzoek is daarom ook sterk aanbevo-len.

Het tweede deel van dit proefschrift beschrijft het ontwerp en de realisatie van een me-chanisch-optische modulator. Hierbij is gebruik gemaakt van een hybride integratie-techniek, waarbij een optische golfgeleider chip en een mechanisch modulator-element afzonderlijk van elkaar zijn gerealiseerd en vervolgens zijn geassembleerd. De gebruikte optische golfgeleider chip, TripleX-waveguide genaamd, is ontwikkeld door LioniX B.V. Het modulator-element bestaat uit een lichtgewicht en tevens rigide plaatstructuur van siliciumnitride die verend is opgehangen. Op deze plaatstructuur is een dunne goudlaag aangebracht ten behoeve van de optische modulatie. De integratie van beide delen wordt gerealiseerd door middel van een speciale uitlijntechniek met een maximale uit-lijningsfout van twee micrometer. Om snelle schakeltijden te verkrijgen is er gebruik gemaakt van bi-directionele elektrostatische actuatie, om het mechanische modulator-element zo snel mogelijk van en naar de golfgeleider te bewegen.

Het voornaamste deel van dit onderzoek naar van een mechanisch-optische modulator is gericht op het ontwerp en de optimalisatie van een lichtgewicht mechanisch element dat geïntegreerd kan worden met verschillende optische golfgeleiders. Een belangrijke eigenschap van het mechanische modulator-element zijn de ribbels die ervoor zorgen dat de plaatstructuur rigide is en zodoende vlak blijft. Daarnaast zorgen deze ribbels ervoor dat de statische wrijving minimaal is op het moment dat het modulator-element het sub-

straat raakt, waardoor de plaatstructuur niet blijft kleven. De geïntegreerde me-chanisch-optische modulator is gekarakteriseerd door het uitvoeren van elektrische en optische metingen. Capaciteit-Spanning (CV) metingen laten zien dan de bi-directionele actuatie succesvol gerealiseerd is. Deze metingen laten ook zien dat het mechanische modulator-element vlakbij de golfgeleider gebracht kan worden en dat de gebruikte uit-lijntechniek succesvol is. Om ook de mechanisch-optische modulatie zelf te kunnen waarnemen is er een aangepast ontwerp nodig, waarbij het ontwerp van de golfgeleider dient te worden verbeterd.

Preface

The work presented in this thesis was performed within the frame work of the MEMPHIS (**M**erging **E**lectronics and **M**icro and nano **PH**otonics in **I**ntegrated **S**ystems) project which was funded by the Smart Mix programme. The goal of the MEMPHIS project is the research and development of an integrated electronic-photonic technology platform where the focus is given in merging the technologies and to bring the best from the technological worlds. Within MEMPHIS, there are several work packages involved in application specific research to exploit light in medical diagnostics, healthcare, entertainment, telecommunications, tracking and positioning. In which, the underlying technologies are Ultra-fast Signal Processing, Terahertz Imaging, Broadband Communication Technologies, Sensor Technology, Raman-spectroscopy, Laser Imaging and Light Sources.

The aim of the Work Package (C14-Parallel Plates) that dealt in this thesis is to investigate the realization and control of micromachined plates, suspended at extremely small distance above the substrate. Such plates are basic building blocks in many applications, e.g. power sensors, optical modulation using a mechanical structure in the evanescent field, electro-mechanical tuning and electrical and optical switches. The prime focus of this thesis is to realise suspended plates at sub-micron separation distances that can be controlled with sub-nanometre resolution. In MEMS, the use of parallel plate structures dates back to the transistor built by *Harvey C. Nathanson* in 1967 [1]. Since then, parallel plate geometry is widely used in numerous micro devices employing different means of actuation and detection. With parallel plate structures, the displacement in sensors such as micro-accelerometers and gyroscopes can be detected [2, 3]. In Bio-MEMS applications, they are used to actuate the micro-pumps and micro-valves [4, 5], whereas in RFMEMS and optical applications, they are used to tune the capacitance [6], adjust the frequency of a filter [7], and modulate the light beam [8] and scan a laser [9].

The parallel plate structures concept covers a broad spectrum of research involving several fields of interest. Therefore, the research dealt in this thesis was narrowed down by defining the goal of the project. Within the MEMPHIS project the most important application is optical switching in ring based multiplexers and de-multiplexers, in which, an optical modulator is used to switch the optical signals in and out of the ring resonators. Besides, control using a moveable plate using electrostatic actuation instead of thermal actuation significantly increases the achievable switching speed. Depending on the size of the structure, switching speeds in the millisecond to microsecond range are feasible. To this purpose, the integrated optical nano-mechanical (IONM) effect was studied to construct a mechano-optical modulator, which has shown considerable achievements in the past few decades [10-15]. The prime focus of this research was given to the realisation of a fast moving mechanical device that can be used with any waveguide such as optical waveguide, photonic crystals, coplanar waveguides (CPW) etc., to perform the ON-OFF modulation of the signal propagating through it.

Subsequently, the study started with the design and realisation of light weight mechanical structures as switching element. Moreover, a bi-directional electrostatic actuation is used for the movement of mechanical element towards and away from the waveguide. The main concern with the electrostatic actuation with the parallel plate structures is the pull-in instability; which, ultimately results in the stiction of collapsing structures together. To avoid stiction of the suspended plate or the mechanical structure discussed in this thesis, the bottom part of these mechanical structures is designed with ridges that prevent the stiction and also prevents the beam from bending due to residual stress. These mechanical devices are initially realised on wafer scale and are characterised using a Polytec Laser Vibrometer (PLV) and White Light Interferometer (WLI). After successful characterisation of these devices, the mechanical structure to be integrated with the optical waveguide was realised and a novel technique to assemble and bond them was successfully realised. The design, fabrication and characterisation of these mechanical structures, optical waveguide and the optical modulator are discussed in Chapters 6, 7 and 8 of this thesis.

The general desire for ever increasing functionality of MEMS with further decrease in the size of the devices are constantly challenged with the capillary, van der Waals or Casimir forces depending on several other factors such as size of the device, humidity and temperature [16]. The investigation on these forces is active in the past few decades, where considerable increase in their experimental research is emerging since the advent of

MEMS. One of the most contributed researches among the fundamental force investigation is observed on the Casimir force measurements [17-21]. The Casimir force which makes its presence in the absence of any external charge mainly depends on the surface area and the separation distance of the geometry involved [22]. This has been regarded as the macroscopic manifestations of retarded van der Waals interaction.

It has also been discussed that the Casimir force can introduce bending of beams and plates and cause stiction of two parallel plates in close proximity [23]. The Casimir force and its dependence on the boundary conditions of electromagnetic fields is a phenomenon that is mostly avoided rather than explored. Within this parallel plate research, the investigation of Casimir force is also carried out as part of understanding the underlying physics at smaller separations in such geometry. Under this research study, the focus is on the use of parallel plate structures separated at sub-micron distance. A measurement principle using such geometry was devised and fabrication schemes are explored to realise parallel plates separated at a distance of $\sim$1 μm. The first part of the thesis (Chapters 2 to 5) is devoted to the research carried on Casimir force measurement, where the design principle, fabrication procedures to realise the parallel plate geometry meeting the experimental requirements are discussed in detail. Besides, the experiments conducted towards the assessment of the Casimir force between parallel plates are also explained with the results obtained.

Outline of the Thesis

In this thesis, Chapters 2 to 5 present the study performed on Casimir force measurement with parallel plate geometry. Later, in Chapters 6 to 8 the research study on the design and realization towards a fast mechano-optical modulator is described. Though this thesis discusses two different topics, in Chapter 1 it is explained that these two subjects are strongly related to each other. Briefly, the outline of this thesis is given in the following Table.

Thesis Introduction	: Chapter 1
Casimir Force Measurement	: Chapters 2, 3, 4 & 5
Mechano-Optical Modulator	: Chapters 6, 7 & 8
Conclusions & Recommendation	: Chapter 9

Chapter 1 gives an introduction to the topics discussed in this thesis. A background on the development of MEMS is discussed where the significance of parallel plate geometry is highlighted. Challenges faced in further miniaturization in MEMS are also discussed, where the surface level forces play a major role at sub-micron separation distances within the MEMS devices. Casimir force starting from its point of prediction through the zero-point fluctuation is introduced. Later in the same Chapter, an introduction to the mechano-optical modulator based on Integrated Optical Nano Mechanical (IONM) effect is presented, which is also studied in the later part of this thesis.

The experimental studies on Casimir Force Measurement (CFM) has been on go ever since its prediction. There has been constant upgrading of the measurement methodologies since the advent of MEMS. **Chapter 2** a concise history on the experimental studies carried out so far. As the experiments for CFM are performed with real materials and at finite temperature and pressure, the original Casimir force has to be modified to include these correction factors. These corrections factors are also addressed in this Chapter, which are also momentous in the experiment methodology discussed in this thesis.

Chapter 3 describes the principle of measurement methodology involved in the experimental investigation of Casimir force. The design analyses to realise the micromachined parallel plate geometry is discussed in detail. Different ways to measure the Casimir force is devised based on the principle presented and are explained with the theoretically predicted results.

In **Chapter 4**, the fabrication processes to develop the parallel plate structures are presented. The main objective is to realise plates separated at sub-micron distance. For which, two different fabrication schemes involving two different bonding techniques are developed. The characteristics, optimization, drawback and complexity of the fabrication steps are discussed in detail. In the end, a comparison between two fabrication schemes is also given.

Chapter 5 presents the results from preliminary experiments performed on the verification of Casimir force. Initial characterisation of the fabricated devices in a vacuum environment indicates that the devices behave as expected. The initial characterisation of the realised plates for surface roughness and waviness are also presented in this Chapter.

Chapter 6 introduces the design of the mechano-optical modulator based on IONM effect. The prime focus here is the realisation of light-weight mechanical device as switching element in the modulator. In this Chapter, the design of the mechanical element, optical waveguide and the hybrid integrated mechano-optical modulator are discussed.

Chapter 7 presents the fabrication schemes to realise the mechanical element, optical waveguide and ultimately the assembly procedure to perform the hybrid integration of mechanical chip with the optical chip. With successful characterisation of the mechanical element, the final design of the optical modulator was devised and developed.

Chapter 8 discusses the experimental results obtained from the characterisation of mechanical and optical devices that constitute the modulator. Prior to integration, both the mechanical structure and optical waveguides underwent series of tests and measurements and their results are also discussed in this Chapter. After individual characterisation and measurements, the hybrid integrated modulator is exploited for both electrical and optical measurements. The results of the experiments with the integrated device along with the additional modelling of the performance of the integrated device based on the information extracted from the measurement results are also discussed.

In **Chapter 9**, conclusions on both the topics based on their experimental results are presented. An outlook on the future prospects of the use of these parallel plate structures for the investigation of the Casimir force is also presented. For the mechano-optical modulator, further improvements with respect to design and experiments are also discussed.

The fabrication processes devised and used in the realisation of the parallel plate structures for both the Casimir force measurements and the optical modulator design are given in appendices A, B, C & D.

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Chapter 1

Introduction

Synopsis

An introduction to the topics studied in this thesis is presented in this Chapter. Background on the development of MEMS is discussed where the significance of parallel plate geometry is highlighted. Challenges faced in further miniaturization in MEMS are also discussed, where the surface level forces play a major role at sub-micron separation distances within the MEMS devices. A brief introduction on the Casimir force starting from its point of prediction through the zero-point fluctuation is given. Later, an introduction to the mechano-optical modulator based on Integrated Optical Nano Mechanical (IONM) effect is presented, which is also studied in the later part of this thesis.

Over the centuries of discovery and development in scientific field, it has been always by looking into the mysteries of nature that all the inspirations and eureka moments unfolded. Right from the era of *Stone Age* to the present day, the need for the sustenance of life in this planet has lead to many inventions and discoveries through the understanding of natural world (science) and the ability to manipulate it (technology). So far, the world has seen tremendous amount of changes in terms of the evolution of new technologies and the resulting applications have become an invaluable part of day-to-day lives of human being.

In the last few decades, the most evolving growth is seen in the field of Micro-Electro-Mechanical Systems (MEMS), which is basically made of electrical and mechanical components scaled down to micrometer dimensions. The history of miniaturization dates back to the invention of the first electrostatic motor by *Benjamin Franklin* and *Andre Gordon* in 1750's. Later with the advent of silicon in 1824, the development in this field has been inching until the commercial silicon strain gauges are made available in 1958. Since then the scientific world has been witnessing successive growth in this field. Though the development of MEMS technology is through the integrated circuit (IC) industry, there has been significant growth in the MEMS field as self-governing machinery.

The speciality of MEMS technology is in the prospect of bringing different fields of science into one common abode that resulted in the realisation of various sensors and actuators that routinely underwent further miniaturisation. Most of the microstructures that find application in sensing pressure, power and force are designed with the geometries having large surface area with relatively small separation distance between them [1-3]. Devices with such geometry are generally referred as parallel plate actuators or sensors [4,5]. Ever since the discovery and use of MEMS technology, parallel plate actuators have been of great importance in MEMS field for numerous applications as mentioned before.

Scaling down the dimensions in one way allowed the possibility to increase the number of devices on a given area; on the other hand it was entering the area where the surface level forces and fields ruled everything around them. Continuous miniaturization of the MEMS devices should be dealt with the appropriate understanding and control of the physical systems behaviour on these scales. The understanding of fluid, electromagnetic, thermal and mechanical forces on micron length scale are essential to comprehend the operation and function of MEMS devices.

1.1 Quantum Fluctuations and their Manifestations

Through fundamental forces, all the elementary particles in nature interact with each other. These fundamental forces are classified as strong, weak, electromagnetic and gravitational forces. Of which, virtually, every force experienced in everyday life with the exception of gravity is electromagnetic in origin. At atomic scale, the strong forces that hold protons and neutrons together in the atomic nucleus are hundred times more powerful than the electrical forces, however they are short ranged which hinders them being experienced at larger scale. The weak forces, which are not only short ranged but are much weaker than the electromagnetic forces. As for gravity, it is extremely feeble that only with huge concentrated mass (like earth, sun) that it can be noticed. Amongst all, the electromagnetic interaction is overwhelmingly dominant; which is the source of various interactions that determines the properties of liquids, gases and solids and their chemical reactions and biological structures.

In the electromagnetic interactions, there are continuous jostling of positive and negative charges that give rise to transient electric and magnetic fields in a material body and as well in vacuum. Though thermal agitation remains one of the reasons behind the occurrence of such fluctuations, there are other factors that contribute to its presence, even in a vacuum space. These fluctuations are the results of collective contribution of moving electric charges, currents and fields that are averaged over time, which ultimately creates the charge fluctuation forces. In quantum mechanical systems, the fluctuations at their ground state constitute a zero-point energy, which includes different fields such as electromagnetic fields, fermionic fields, and Higgs fields. According to quantum physics, it is the energy that remains when no excitations present in the system. The best example could be taken from the quantum oscillator whose energy level is given as

$$E_n = \hbar\omega(n + \frac{1}{2}) \tag{1.1}$$

where $\hbar = h/2\pi$ is the Planck's reduced constant and ω is the angular frequency and n is an integer. At $n = 0$, there is still the ground state energy, E_0 as given below:

$$E_n = \frac{\hbar\omega}{2} \tag{1.2}$$

It is this ground state energy that contributes to the residual motion of the oscillator,

which always remains due to the requirement of the Heisenberg uncertainty principle.

1.1.1 Casimir Force

One of the most interesting outcomes of quantum vacuum fluctuation is the Casimir force as predicted by *Hendrik G. Casimir* in 1948 [6]. The Casimir force in its original form is formulated between two neutral conducting plates in parallel that are attracted towards each other mainly due to the zero - point energy between them [7, 8]. The cavity between such plates cannot sustain all modes of the electromagnetic field. In particular wavelengths comparable to the plate separation and longer are excluded from the region between the plates. This fact leads to the situation that there is a zero-point radiation overpressure outside the plates which acts to push the plates together. It has the property of increasing in strength with the inverse fourth power of the plate separation, d^4. The force diverges when elements of the plates come into contact, where the surface smoothness of the plates becomes a limiting factor. In other case, when the plates are so close that the corresponding zero-point radiation wavelengths no longer feels a perfectly conducting surface. The non-continuous nature of the plates, as opposed to the true surface and molecular nature of the materials, becomes an important factor for very short distances.

Under ideal conditions such as plane parallel geometry, perfectly conducting and ideally reflecting material at zero temperature surroundings, the Casimir force turns out to be[6]:

$$F_C(d) = \frac{\pi^2 \hbar c A}{240 d^4} \tag{1.3}$$

which depends on the separation distance, d and the surface area of interaction, A. The only fundamental constants that enter the equation are $\hbar$ - Planck's reduced constant and c velocity of light.

Figure 1.1 presents the quantitative value of the increasing force for two different interacting or overlap areas of the plates. The Casimir force can increase up to 1 atm pressure for a separation distance of 10 nm [9]. From this, it can be inferred that micromachined devices could noticeably produce macro level pressures and measurement of such forces could result in exploring interesting phenomena underlying there. The growth in the experimental investigation of the Casimir force is increasing along with MEMS field [10-16]. As seen by every other major discovery such as electricity in 17^{th} century and computer in 20^{th} century, the development in the Casimir effect is also unpredictable. The practical use of this effect is still underway, which will possibly lead to intelligible devices to make

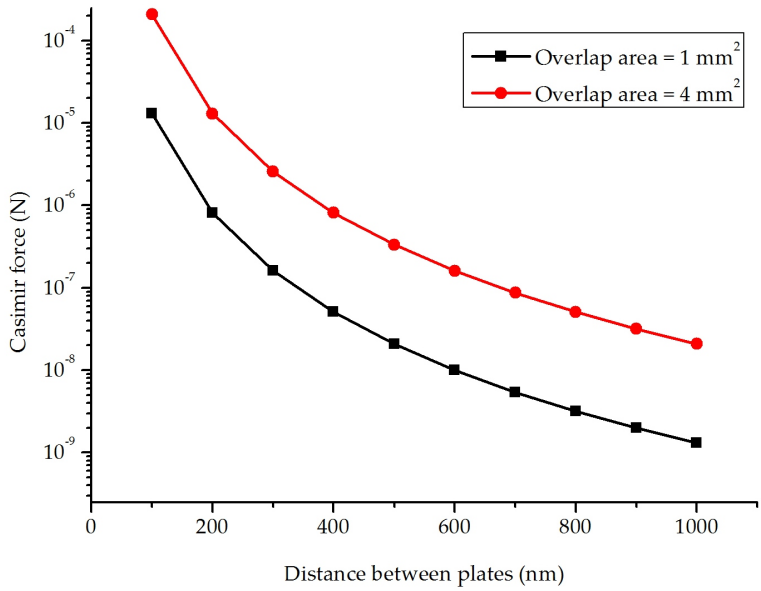

Figure 1.1: Casimir force variation with increasing separation distance for two different overlap areas

use of this effect and avoiding the consequences of this effect. For further development in MEMS field, the understanding of the Casimir effect at such scale will not only overlay new methodologies, but will also help in improving the yield of the MEMS and NEMS devices.

1.2 Integrated Optics

The ever increasing demand of high speed internet connection and data communication in the last few decades have ensured the possibility of enabling fibre optical data communication as a great alternative to the electrical communication. The developments in the fibre optical communication have encouraged the demand for compact and cost effective optical devices. Optical Integrated Circuits (OIC) have the potential to enhance the functionality of optical systems, lower the manufacturing cost and complexity of fabrication as similar to what has been achieved by integrated electronic circuits. The need for compactness has also lead to the need for better reliability, better mechanical and thermal stability, low power consumption and low drive voltages in active devices. Besides, the vision for OICs is the integration of different functionalities such as lasers, modulators, filters and optical switches in one common package.

One important application in optical communication is the optical modulators and switches. These switches and modulators are involved in multiplexing/de-multiplexing, optical beam steering, reconfigurable interconnect and switch selectable time delay networks [17-21]. These devices can be achieved by using electro-optic materials ($LiNbO_3$), acousto-optic materials, and ferroelectric liquid crystals. However, passive materials are also be used to create such functionalities. The prime advantages of the passive materials usage in integrated optics is low loss, lower index of refraction, compatibility with fibre optics and ability to be fabricated using standard integrated circuits materials such as Silicon (Si), Silicon dioxide (SiO_2) and Silicon nitride (Si_3N_4). The required change of index is however achieved externally. This also provides the possibility of integrating optics with electronics and mechanics. One of the outcomes of integrated optics is the Integrated Optical Nano Mechanical effect (IONM) [22]. Unlike thermo-optics materials, devices based on IONM effect does not require large power consumption for switching operation. Both intensity and phase modulation are possible with this effect.

1.2.1 Mechano-Optical Modulator

Ever since the prediction of the integrated optics, the IONM devices find more suitable applications in the realm of telecommunication applications where micro to millisecond response times is sufficiently fast. The IONM effect is performed by changing either the real or imaginary part of the effective refractive index of the guided mode. In which the mechano-optical interaction is achieved by moving a mechanical element in the proximity of the optical waveguide so that it can perturb the evanescent field of the waveguide mode [22].

Several devices have been reported based on this effect such as Mach-Zender based 1x2 switch [23], wavelength tuneable Bragg reflectors [24,25], and acousto-optical sensors [26]. All these devices are based on the phase modulation, performed by moving an optically transparent material in and out of the evanescent field that results in the modulation of the real part of the refractive index.

Electrostatically actuated ON/OFF intensity modulator by using an absorbing material is also realized [27]. In which the modulation is achieved by introducing absorption loss into the optical path. Such modulator behaviour is non-periodic and the extinction that can be obtained is very high, in the order of 37 dB. An advantage is that no actuation is required in the ON state.

The basic principle of IONM effect is shown in Figure 1.2 The air gap d, between

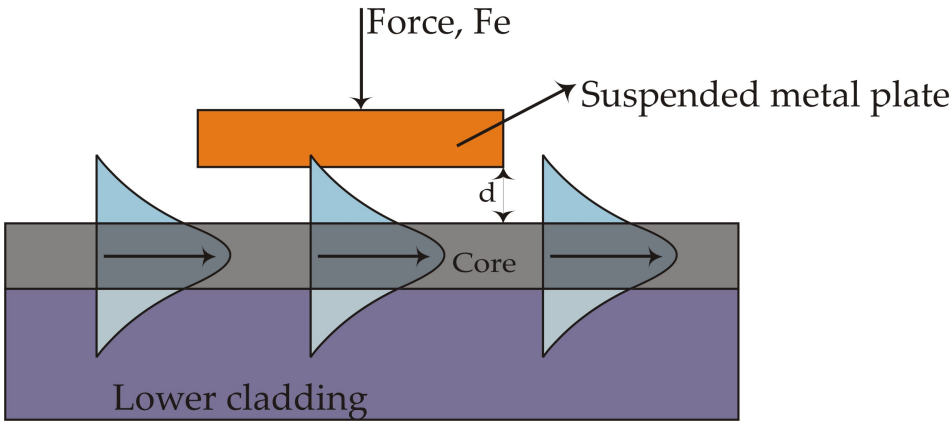

Figure 1.2: Principle of evanescent coupled mechano-optical modulator

the mechanical element and the optical waveguide is varied by the electrostatic force between them. When the air gap is considerably less than the wavelength λ, ($d \leq \lambda$), the evanescent part of the guided wave penetrates through the gap into the mechanical element, thus changing the effective refractive index (N) of the guided mode. A small change in the air gap Δd, can introduce significant changes in the ΔN that are sufficient for the operation of the IONM devices.

The force required to actuate the mechanical structure which can be a cantilever, bridge or membrane is obtained by, for example electrostatic, piezoelectric, electro-dynamic, thermal or mechanical forces. The use of electrostatic actuation amongst other actuation schemes has shown more possibility in achieving fast responding switches and modulators. Further, no actuation is needed in the ON state of the switch or modulator, while the actuation requires low power consumption [28, 29].

In the second part of the thesis, focus is given on the realisation of light-weight mechanical structures that could ultimately be used on any waveguide to perturb the signal propagating through it in micro-second duration. Using this mechanical device, both phase and intensity modulation based on the IONM effect is possible. The mechanical element is fabricated in silicon rich silicon nitride (SiRN). For the intensity modulator, a metal layer is deposited on the SiRN beam which introduces the absorption loss into the optical path to perform as ON-OFF intensity modulator.

1.3 References

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Chapter 2

Casimir Force for Real Materials: Experimental Background

Synopsis

The experimental background on the Casimir force measurements are discussed in this Chapter. A brief background on the existence of the Casimir force is presented in section 2.1. An introduction to the Lifshitz formula, which describes the Casimir force for real materials, is given in section 2.2. Since the original Casimir force was derived for the ideal mirror properties of the materials and ambiences, to compare the measured result with the theoretical values, the formula needs to be modified. Various correction factors that need to be added in the Casimir force theoretical calculation with respect to the material properties and experimental conditions are discussed in Sub-sections of 2.2. A summary of various experiments on the measurement of Casimir force is presented in section 2.3. Here, the importance of each experiment with respect to the precision level that has been achieved is also highlighted. In section 2.4, a brief description of the measurement method investigated in this thesis is presented. The summary and discussion of this Chapter are presented in Section 2.5.

2.1 Background

In 1948, *H. B. G. Casimir* while working in Philips Research Laboratories, Eindhoven discovered the Casimir effect [1]. His frequent discussions with *Niels Bohr* led him to focus on the zero point energy. Fluctuations in quantum vacuum of the electromagnetic fields within the cavity formed by two conducting plates in parallel acting as perfect mirrors lead to an attractive force. Inside the cavity, only the modes that fit half-integer number of wavelengths are allowed whereas outside of the cavity, all possible modes can exist. Owe to this reason the radiation pressure from outside is larger than that from the inside and as a result, the plates attract each other. Besides, long range interactions such as those between atoms or molecules (van der Waals interaction), atom and material surface (Casimir-Polder interaction) and attraction between bulk material boundaries are also termed as Casimir effect [2].

For ideal conducting flat parallel plates at zero temperature with an area A, the magnitude of the Casimir force is given by following equation [1]:

$$F_C(d) = \frac{\pi^2 \hbar c A}{240 d^4} = \left(\frac{A}{1mm^2}\right)\left(\frac{d}{100nm}\right)^{-4} \cdot 13.02\mu N \tag{2.1}$$

Equation 2.1 depends on the separation between the plates, d and fundamental constants such as Planck's reduced constant ($\hbar$) and the speed of light in vacuum (c). The force described in equation 2.1 is based on ideal properties of material bodies and the environment conditions. For real materials, Equation 2.1 should break down for small d, as at such small separation distances, the mode frequencies are higher than the plasma frequency , ω_p (for metals) or higher than the absorption resonances (for dielectrics) of the material used to make the plates [2]. The theoretical work on the Casimir effect far outweighs the experimental research. Only a few dozen experimental results were published compared to about thousand theoretical papers on the Casimir forces. However, *Casimir's* idea remains important among both theoretical and experimental physicists, as evident from Figure 2.1, which shows that the number of citations of the original *Casimir* paper has been increasing quite rapidly with time. This also substantiates the importance of the Casimir effect in various fields of modern physics and engineering.

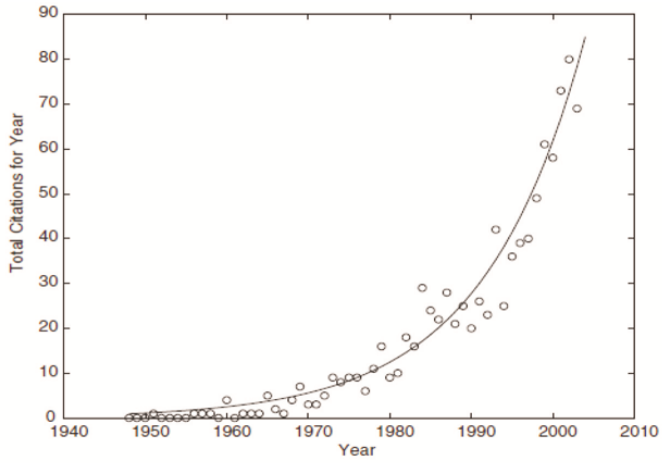

Figure 2.1: Number of citations of Casimir's paper Vs year [2]

2.2 Casimir Effect for Real Materials

2.2.1 Lifshitz Formula

In 1956, *Lifshitz* developed the theory that accounts for the real optical properties of the materials and finite temperature [3]. Within this theory it is recognised that the Casimir and van der Waals forces are the long and short distance limits of one and the same force, which is called the Casimir-Lifshitz (CL) force. This theory describes a material from the macroscopic point of view. This is because the force is important at distances much larger than interatomic distance [3]. The result also stressed the importance of the boundaries and eliminated the possibility of the pair interactions in the limit of high density of boundaries. In summary, this force originates from the fluctuating electromagnetic field produced by the plates [3, 4].

According to this theory, the force between two parallel plate structures (considering two plates as body 1 and 2) separated by a distance, d is defined as [5]:

$$F_L = F(\epsilon_1, \epsilon_2, T, d) \tag{2.2}$$

Where ϵ_1 and ϵ_2 are the dielectric function of body 1 and 2 respectively and T is the absolute temperature.

The Lifshitz formula (LF) can be represented as an integral over either real frequencies (ω) or imaginary frequencies ($i\zeta$). The real frequency representation is given by the

following equation:

$$F \to 0 \text{ if } T \to 0,\ F(T,d) = \frac{\hbar}{2\pi^2}\int_0^\infty dw \coth\left(\frac{\hbar\omega}{2kT}\right) \cdot Re\left[\int_0^\infty dQQk_0 g(Q,\omega)\right] \quad (2.3)$$

where the wave vector in the gap is $K = (Q, k_0)$ with the z-component given by:

$$k_0 = \sqrt{\frac{\epsilon_0 w^2}{c^2} - Q^2} \quad (2.4)$$

The function $g(Q,\omega)$ is given by:

$$g(Q,\omega) = \sum_{\nu=s,p} \frac{1 - D_\nu}{D_\nu} \quad (2.5)$$

where

$$D_\nu(Q,\omega) = 1 - r_1^\nu r_2^\nu e^{2ik_0 d} \quad (2.6)$$

Here $r_{1,2}^\nu$ are the reflection coefficients of the inner surfaces of the plates for two different polarisations:

$$\nu = \begin{cases} s, & \text{or transverse electric (TE) polarization} \\ p, & \text{or transverse magnetic (TM) polarization} \end{cases}$$

The factor $g(Q,\omega)$ describes multiple reflections from the inner surfaces of body 1 and 2. The frequency dependent factor $\coth[\hbar\omega/(2kT)]$ originates from the fluctuation-dissipation theorem.

Equation 2.3 is expressed in terms of integral over real frequencies, which in many cases is not convenient for calculations. This is solved by the contour rotation in the frequency complex plane, which is possible due to the analyticity of the integrand. With this rotation, the force can be expressed as an integral over imaginary frequencies. Contribution to the integral gives only the poles of $\coth(\hbar\omega/2kT)$ located at:

$$\omega_n = i\zeta_n = i\frac{2\pi kT}{\hbar}n \quad (2.7)$$

where $n = 0, 1, 2, \cdots$ and ζ is the imaginary frequency. After introducing this transformation, the LF is expressed in terms of imaginary frequencies as:

$$F \to 0 \text{ if } T \to 0,\ F(T,d) = \frac{kT}{\pi}{\sum_{n=0}^{\infty}}' \int_0^\infty |k_0| g(Q, i\zeta_n) Q dQ \quad (2.8)$$

Here $|k_0| = \sqrt{\epsilon_0 \zeta_n^2/c^2 + Q^2}$ and the function $g(Q, i\zeta_n)$ is not oscillating anymore unlike the function $g(Q, \omega)$ expressed for real frequencies in which the oscillatory effect is due to the factor $e^{ik_0 d}$. The LF is also applicable for the calculation of CL force in all separation distances.

2.2.2 Correction Factors

The Casimir force in its original form is deduced for ideal mirror properties of the metals and at zero temperature and vacuum ambiences. In reality, it is difficult to achieve perfect conductors having infinite conductivity and having perfect reflections for all frequencies. The fluctuations due to finite temperature also play a role in quantifying the Casimir force. Further, most of the experiments dealing with the measurement of the Casimir force are carried out at non-zero temperature and between the deposited metals having finite conductivity and roughness. In such cases, it is important to include the correction factors that take account of these effects and as well the experimental condition. The Lifshitz theory takes into account the real optical properties of materials and finite conductivity of metals and finite temperature involved in practical experiments. However, it does not account for the roughness of the surfaces involved.

The CL force becomes operative at distances smaller than 100 nm, where it becomes comparable with the electrostatic force. At separations below 10 nm the Casimir/van der Waals force dominates any other force. In the experiment discussed in this thesis, the corrections to the Equation 2.1 could be due to the roughness of the area under measurement and imperfect reflection of the deposited metal and the finite temperature effects. In the following sections, the modified Casimir force based on the correction factors that are essential and influential in experiments is discussed. The Casimir force measurement between parallel plate geometry depends on the parallelism between the plates, and hence the anomaly due to the non-parallelism should also be taken care of. In addition to the above corrections, the Casimir force is also strongly dependent on the geometry [5-7] and the corrections associated with the geometry are beyond the scope of this research.

Corrections due to Finite Conductivity

At higher frequencies, any metal can become transparent due to the finite conductivity of the metals. Hence there are finite conductivity corrections to the results based on

Equation 2.1. These corrections may contribute in an order of 10-20% of the net result at separations, $d \sim 1\ \mu m$. These are essential when aiming for high precision measurement of Casimir force.

For simple metal, the dielectric constant is given by the following equation:

$$\epsilon(\omega) = \epsilon_0(\omega) - \frac{\omega_p}{\omega^2} \tag{2.9}$$

And the plasma wavelength, λ_p is given by Equation 2.10:

$$\lambda_p = \frac{2\pi c}{\omega_p} \tag{2.10}$$

where ω_p is the plasma frequency of conducting electrons.

The Casimir force Equation defined in Equation 2.1 is thus modified as stated below in Equation 2.11, which include the effect due to finite conductivity [8].

$$F'(d) = F_c(d)\left[1 - \frac{8\lambda_p}{3\pi d} + \frac{120}{4\pi^2}\left(\frac{\lambda_p}{d}\right)^2\right] \tag{2.11}$$

However, this equation is valid only when $\lambda_p/d \ll 1$; and the Casimir force is large enough to be measured accurately experimentally only in the range $\lambda_p/d \approx 1$ or larger. This implies that the measurement of reduced Casimir force due to finite conductivity corrections require more sensitive experimental set-up when compared to the perfect metals.

Corrections due to Rough Surfaces

The interacting surfaces when polished to nearly ideal optical reflection can still have roughness on their surfaces in the order of nano-meter. From the earlier experiments, it was observed that surface roughness increases the actual Casimir force, leading to systematic errors in the measurement [9-11]. The surface roughness also introduces a lower limit on the separation distances between the interacting bodies [12]. In the proximity force approximation [22, 23] the Casimir force incorporating the roughness correction is given by:

$$F'(d) = F_c(d)\left[1 + 4\left(\frac{A}{d}\right)^2\right] \tag{2.12}$$

where A is the root-mean-square (rms) roughness. This formula is applicable if $A \ll d$and the lateral size of roughness L (correlation length) $L \gg d$ [11]. In general, both evaporated

and sputtered thin films have inherent roughness due to their deposition conditions, grain growth and the properties of the substrates. To estimate the effect of surface roughness on the Casimir force at small separations, proximity force approximation cannot be used and more elaborate approaches are needed. The approach taking into account the roughness effect perturbatively was developed in [13, 14]. A possibility to include high peaks that cannot be treated perturbatively was developed in [13]. Local surface slopes arising from the roughness of the thin films also contribute to the Casimir force at very small separations [15]. This is due to the scattering of the electromagnetic waves at the localized rough regions. The roughness corrections also play a crucial role in the estimation of the lateral Casimir force [15].

Corrections due to Finite Temperature

At non-zero temperatures, the fluctuations arise not only from quantum mechanics but also from thermal effects. The Casimir effect at finite temperature is interesting in terms of the present experimental condition, where most of the experiments are performed at non-zero temperatures. Its temperature dependence was first reported by Lifshitz *Lifshitz* [3]. Later further explored by *Fiertz, Sauer* and *Mehra* [16-18] for conducting planes with a contradictory result that differ from the Lifshitz result by the factor of 1/2 in the high temperature limit [19].

For the measurements aiming below 2 μm separation distance, the effect due to temperature can be negligible and is therefore not taken into account. This is because at room temperature, the thermal wavelength can be calculated as [5]:

$$\lambda_T = \frac{\hbar c}{kT} = 7.6\ \mu m \tag{2.13}$$

When $d \ll \lambda_T$, the contribution of the zero-point fluctuations dominates over the thermal fluctuation and hence it can be neglected [20]. Wherein the opposite limit $d \gg \lambda_T$, the thermal contribution is dominating. In such case, only $n = 0$ term is important in the sum of Equation 2.8, because when $n = 0$ corresponds to $\zeta \to 0$. With this simplification, the force equation given in Equation 2.8 becomes:

$$F(T,d) = \frac{kT}{160\pi d^3} \int_0^\infty \frac{x^2 dx}{\frac{(\epsilon_{01}+\epsilon_{00})(\epsilon_{02}+\epsilon_{00})}{(\epsilon_{01}-\epsilon_{00})(\epsilon_{02}-\epsilon_{00})} e^x - 1} \tag{2.14}$$

And this is called the Lifshitz force. The thermal force Equation 2.14 is dominant at

very large separation distances (d) when the force itself is very weak. It should be noted that in the limit $d \gg \lambda_T$, the force is purely classical (no $\hbar$ dependence) because it is a purely thermal effect. Weakness of the thermal force makes it not very interesting for MEMS and NEMS since at separations where the effect of the dispersive forces becomes appreciable the thermal component typically can be neglected [20].

2.3 Summary of Experiments on Casimir Force Measurements

In this section, the experimental development in the measurement of Casimir force is reviewed. Since there have been few attempts made in experimental verification, older experiments are also discussed here, which has set the bench mark and allowed for further improvements. Before one performs the measurement of Casimir force, there are many factors that need to be addressed. The force strongly depends on the separation distance between the bodies used; hence an accurate determination of separation distance is crucial to compare the measured force with the estimated values. Further, the force of attraction is sufficiently strong to be experimentally detected at $d \sim 1000$nm or less, at which the frequencies of interest are in the infrared and optical ranges. Thus an accurate theoretical description of an experimental system must take into account the optical properties of the plate material used.

All recent techniques employed for the measurement of the Casimir force particularly between metallic films were developed by *van Blokland and Overbeek* [21]. Compared to dielectric films, measurements between metallic films pose difficult problems. In the case of dielectric films, optical techniques can be used for alignment and distance measurements. And for metallic films, the distance is determined by measurement of the capacitance between the plates. For simplification purposes, alignment is done by making one plate convex, in which case the geometry is fully determined by the radius of curvature, R at the point of closest approach, and the distance between the plates, d at that point. This technique was first presented by *Derjaguin* [22] and has found broader application as the proximity force theorem [23].

Although a complete review of all the experiments would be quite extensive, here only those notable experiments that have been regarded as landmark in the history of the Casimir force measurement are discussed. There have been many review articles and books published on account of experimental and theoretical development on Casimir

effect [8, 24-27]. Essentially all of the early experiments (before 1980) relied on the use of cantilever balances, and generally produced data such that the $1/d^n$ force law could be determined to roughly 50% accuracy (in n). Lately, piezoelectric actuators replaced the use of balance to automatically control the plate positions. This resulted in the elimination of the mechanical hysteresis observed in the earlier experiments.

2.3.1 General Requirements for the Casimir Force Measurements

Although the existence of Casimir force was predicted in 1948, it was a decade later that the first experimental attempt was made [19]. The experimental technique was based on spring balance and parallel plates made of metals. This experiment sets the bench mark and also showed that the presence of quantum vacuum fluctuation not contradicting the theory. It has also clarified on the various requirements in performing a precise, reliable and reproducible measurement of the Casimir force. The fundamental requirements which are essential for the measurement are stated below [19, 24]:

- Surfaces should be free of dust particles and chemical impurities.
- The measurement of separation distance between the bodies should be done in a precise and reproducible technique.
- The electrostatic charges on the surface and the potential differences between the surfaces should be kept low.

2.3.2 Experiments between Parallel Plates

The very first attempt on measuring the Casimir force was made by *M J Sparnaay* in 1956 [19]. He used spring balance method to measure the Casimir force between two metallic mirrors separated at a distance larger than 1 μm. The sensitivity of the spring balance was (0.1 - 1) x 10^{-3} dyn. The deflection of the spring was measured in terms of the capacitance formed by the two flat plates. Calibration of this capacitance was done with the help of tungsten and platinum wires, uncertainties associated with them were not reported. Care was taken such that the plates are mounted on surfaces that are electrically insulated from the rest of the experimental set-up. It was noted that even a small potential difference of about 17 mV between the plates could disturb the experiment.

The two plates were first brought in contact together in order to avoid any potential difference between the surfaces. Three sets of metal plates; AluminiumAluminium, ChromiumChromium and ChromiumSteel were used in the measurements. Though different electrical and mechanical means of cleaning procedures were in use, the dust particles larger than 2-3 μm were observed on the plates. The alignment of the plates was done with visual inspection with 10% variation in the inter-plate distance from one of the plate to the other. Due to the presence of the dust particles it is estimated that even on contact, the plates are separated by 0.2 μm. An attractive force was observed between Chromium-Steel and Chromium plates, whereas a repulsive force was observed between Aluminium-Aluminium plates. The reason for the repulsive force between aluminium plates was thought to be due to the presence of impurities on their surfaces.

It can be concluded that these measurements confirm the verification of Casimir force between metallic surfaces, which are in agreement with the theory. In these experiments, since the aluminium plates showed repulsive force, the attractive Casimir force was thus not conclusive. The most severe drawback of this measurement technique was due to the difficulty in the determination of separation distance between the plates. From these experiments, *M J Sparnaay* pointed out the problems that needed to be addressed for a rigorous and conclusive measurement of the Casimir force.

2.3.3 New Era in Casimir Force Measurements

The era of high precision measurements of the Casimir force began after almost half century later its prediction. Meanwhile, numerous theoretical modelling considering the roughness and finite conductivity corrections [28-30], temperature corrections [31-33] and geometrical dependence of the Casimir force were performed [5-7]. It was only in 1997 that the first precise measurement of the Casimir force was performed by *S Lamoreaux* [34]. This experimental measurement remains a landmark as being the first in the modern phase of Casimir force measurements. The measurement setup involved a balance based on torsion pendulum, which is made of gold coated spherical lens and a flat surface.

Figure 2.2 shows the schematic representation of the measurement set-up used by S Lamoreaux. In this experimental setup, the plates consisted of quartz optical flat measuring 2.54 cm in diameter and 0.5 cm in thickness and a spherical lens with a curvature radius of 11.3 cm and diameter of 4 cm. Later these surfaces are coated with 0.5 μm thick copper (Cu) through evaporation followed by 0.5 μm of thick gold (Au) layer. The flat electrode was mounted on one arm of the torsion pendulum whereas the spherical

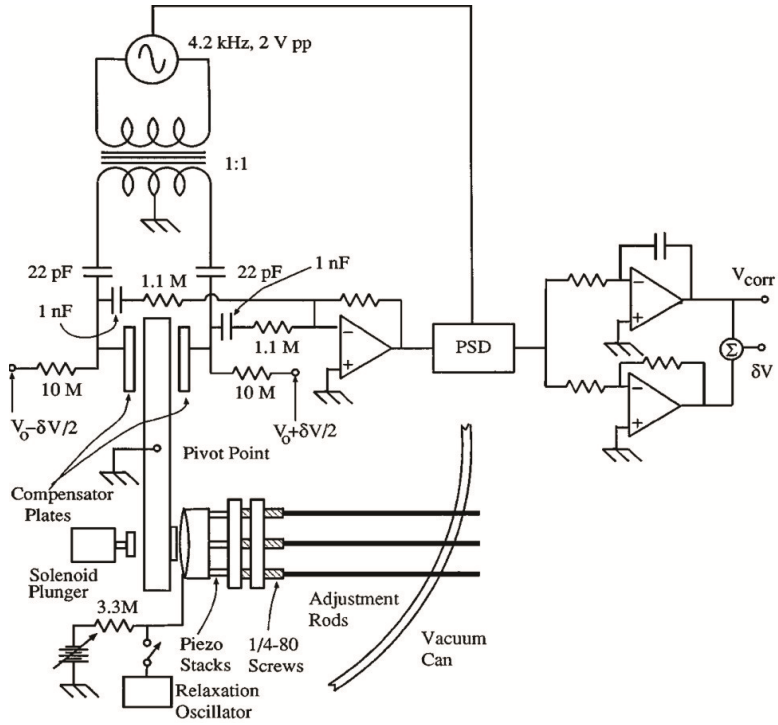

Figure 2.2: Schematic representation of the apparatus used by Lamoreaux for Casimir force measurement [34]

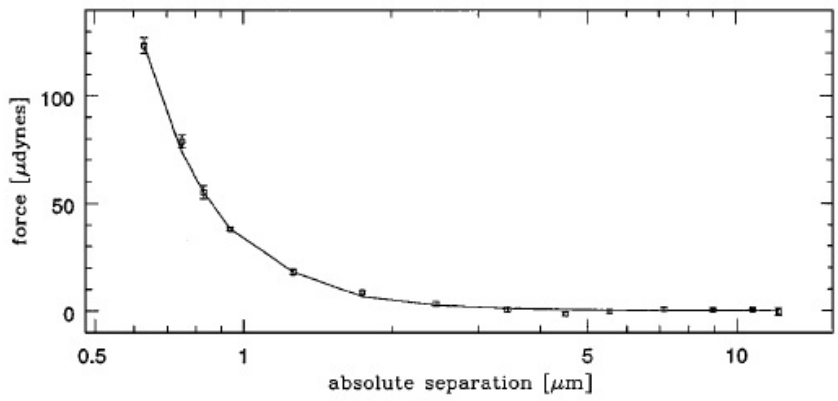

Figure 2.3: Variation of Casimir force with separation as measured in S Lamoreaux experiment [34]

lens is attached to the piezoelectric stack. Adjustment rods attached to the piezoelectric stacks were used to position the spherical lens with 0.5 μm accuracy. A pressure of 10^{-4} torr was maintained inside the measurement chamber. The fixed angle of the torsion pendulum was kept constant with the feedback system. Two compensator capacitors (as shown in Figure 2.2) with the pendulum body provide the feedback signal to the phase sensitive detector in the feedback system. A strong magnet was used to over-damp all the vibration modes of the pendulum. Casimir force measurements were performed by step wise increase in the voltage to the piezo electric stacks. The measured restoring force is directly proportional to the voltage applied to the compensator which kept the fixed torsion angle of the pendulum. Figure 2.3 shows the measured Casimir force which varies with the distance between the spherical lens and the flat plate.

In Figure 2.3, it is also shown that the Casimir force is insignificant at large separations and increases drastically at minute separations. The force shown here is the residual force after subtracting all the electrical forces from the total force. The separation for the closest approach between the bodies is 0.6 μm. Efforts to measure the force beyond the closest approach were hampered by the dirt and instability in the feedback system. The measurements had an accuracy on the order of 5%. The data was not sufficient to prove the finite temperature corrections. The plasma frequency of the Au metallization provides a finite conductivity correction factor of 20% at close spacing, and was also not supported by the measured data. However, this experiment has provided a good platform for the success of precision measurements.

2.3.4 Experiments with Atomic Force Microscope (AFM)

More precise and definite measurements of Casimir force using Atomic Force Microscope (AFM) were carried out by *Mohideen* and *Roy* in 1998 [35], *Roy et al.* in 1999 [36] and *Harris et al.* in 2000 [37] in three successive experiments. In these experiments, the fundamental requirements set forth by *M J Sparnaay* were met for the first time. With the use of AFM tip the Casimir force was measured between a metallic sphere and flat plate. The schematic representation of the experimental set-up is shown in Figure 2.4. Casimir force between the sphere and the plate would result in the bending of cantilever. This bending is detected by the deflection of a laser beam leading to a difference signal Δ_{def} between photodiodes A and B which was calibrated by means of the electrostatic force between the sphere and the plate.

To measure the Casimir force between the sphere and the plate, they are both

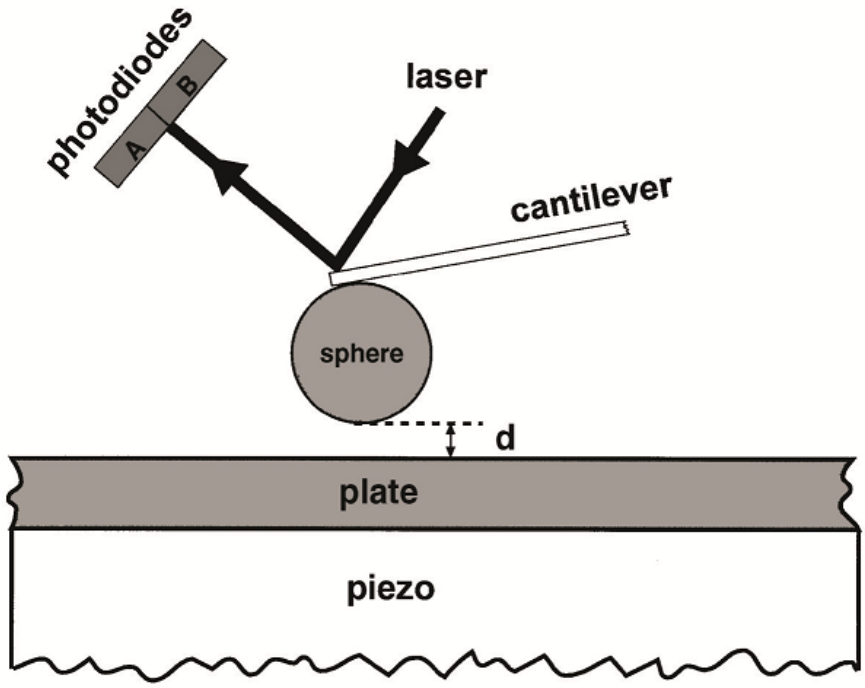

Figure 2.4: Schematic of the measurement using AFM tip used by Harris et al., [37]

grounded together with the AFM. The plate is then moved toward the sphere using the piezo and the corresponding photodiode difference signal is measured. It is then converted into the respective deflection of the cantilever tip and by use of Hooke's law into the values of the Casimir force $\Delta_{def}km$, where k is the spring constant.

In the first two experiments performed by *Mohideen* and *Roy* [35] and *Roy et al.* [36], the sphere, made of polystyrene and the plate are first coated with 300 nm of Al and then sputtered with layers of Au/Pd to avoid rapid oxidation of Al. In these experiments, they have reported a statistical precision of 1% at the smallest separations in the measurement of the Casimir force. The measurements were performed in smaller distances of separation ranging from 0.1 μm to 0.9 μm.

Figure 2.5 shows the results from the AFM tip measurements performed by *Mohideen* and *Roy* in [35]. The measured Casmir force values are shown as square dots in the Figure 2.5. The solid line shows the theoretical value of the Casmir force with finite conductivity, roughness and temperature corrections. The rms deviation between the measured and the theoretical values was 1.6 pN which is less than 2% error at the closest approach. This experiment proved the possibility of the precision measurements using the miniaturised

devices.

For straightforward purpose with the theoretical predictions, *Harris et al.* [37] measured the force between bodies covered with deposited Au. Using gold coated surfaces eliminated some uncertainties in the interpretation of measurements. Complete dielectric spectrum of metal was used in comparing theory with the experimental results. However, the average statistical precision remains at the same 1% of the forces measured at the closest separation.

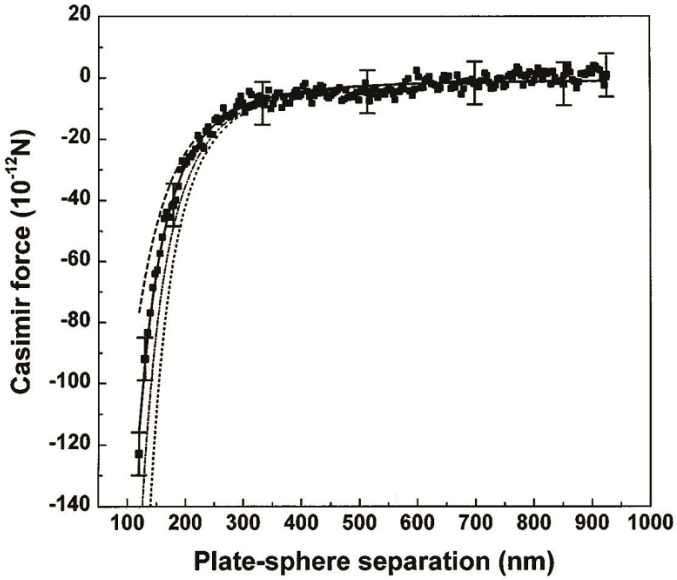

Figure 2.5: Results from Casimir force measurements using AFM tip by Mohideen et al., [35]

2.3.5 Experiment Using Cylinder-Cylinder Geometry

In another experiment by *T Ederth*, crossed cylinders were used as device geometry to measure the Casimir force [8]. The template stripped macroscopic gold surfaces were used for the measurement of the Casimir forces between 20 nm to 100 nm range. Specially prepared gold surfaces were mounted on the two cylindrical bodies with the top surface showing gold. The Casimir force measurement setup with the cylinder bodies is shown in Figure. 2.6. The position of the upper cylinder was controlled by the motorized stage and piezoelectric tube whereas the bottom cylinder position was measured by the bimorph actuator. With the use of LVDT (Linear Variable Displacement Transducer)

the expansion of the piezotube was monitored in order to avoid any hysteresis in the subsequent data analysis.

The second cylinder is mounted on piezoelectric bimorph deflection sensor, which acts as the measurement spring. The charge produced by the deflection is measured by the electrometer amplifier. The radius of curvature of the cylinders used was 10 mm. A special cleaning and deposition technique was used to keep the cylinders in a clean and pristine order. This equipment was specially designed for the force measurements in the macroscopic bodies. The position of the piezotubes could be controlled within the accuracy of 50 nm.

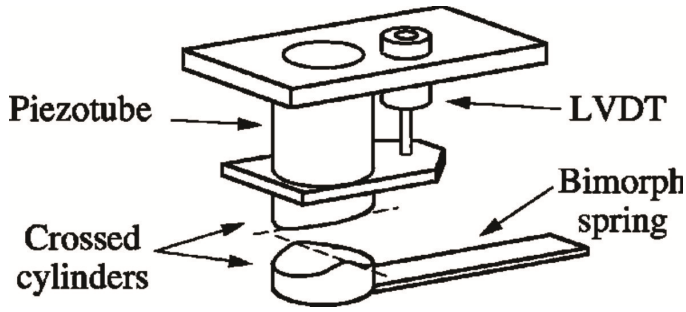

Figure 2.6: Experimental set-up used by Ederth [9]

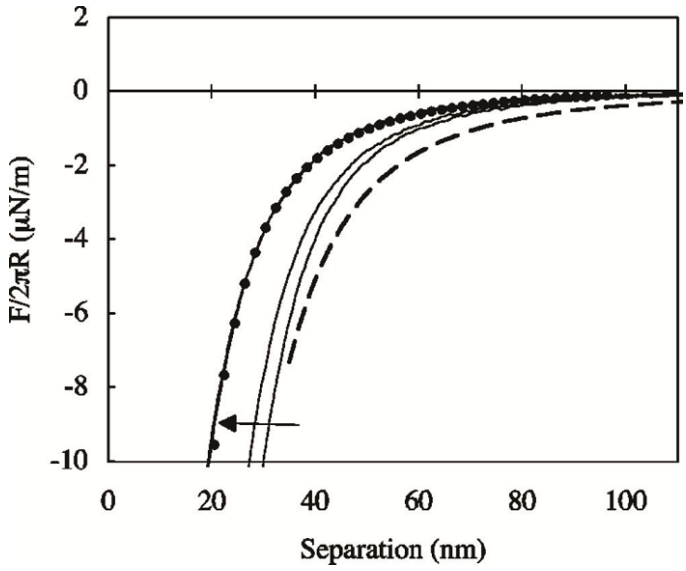

Figure 2.7: Results from experiments performed by Ederth. Solid curves represents the two independent experiments, the dashed line represents the Casimir force [9]

Figure 2.7 presents the force profiles calculated with the average values for two different

experiments [9]. This experiment suggested the use of macro-surfaces for the increased precision of the Casimir force measurements. The results were in good agreement with the Lifshitz theory even after the deformation of the surfaces has taken place.

2.3.6 Experiments Using MEMS Torsional Actuator

In 2001, *H B Chan et al.* made use of a micromachined oscillator to demonstrate the influence of Casimir force on the static and dynamic properties of MEM systems [6]. The measurements were performed between heavily doped polysilicon plate and polystyrene sphere. Both the sphere and plate are evaporated with 200 nm thick Au film with Cr as the adhesion layer. The polysilicon plate was supported by torsion rods which are anchored to the substrate as presented in Figure 2.8. There is a fixed gap of 2 μm between the polysilicon plate and the fixed electrodes, which are symmetrically located underneath it, as can be seen in Figure 2.8. The polysilicon plate was later released over the silicon substrate after etching the silicon dioxide sacrificial layer.

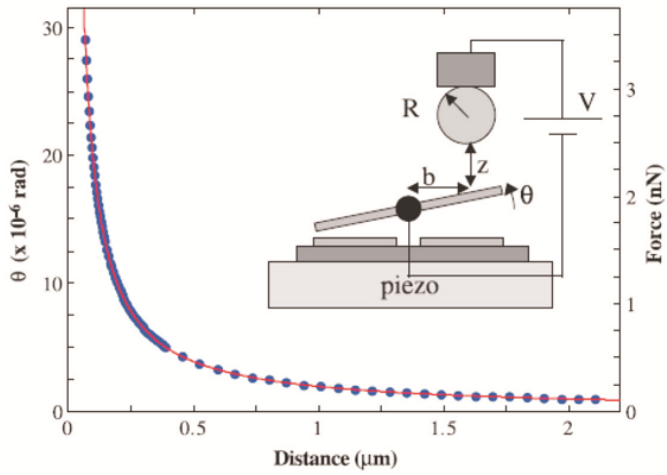

Figure 2.8: Angle of rotation of the top plate due to electrostatic force, also shown is the schematic representation of the experimental set-up used by Chan et al [6]

The rotation of the polysilicon plate about the torsion rods was detected by the capacitance change between the top polysilicon plate and the bottom electrodes. The movement of the polysilicon torsion actuator was controlled by applying minute voltage pulses to the piezoelectric platform, as shown in Figure 2.8. The Casimir force between the metallic sphere and the polysilicon plate caused one end of the plate to tilt further changing the capacitance between the plates and the electrodes. Figures 2.9 (a) and 2.9

(b) show that the torsion angle of rotation and the magnitude of the Casimir force were increased abruptly as the separation between the bodies is below 0.5 μm.

Figure 2.9 (a) shows the Casimir force (red) and electrostatic force (green) superimposed on the same graph. Figure 2.9 (b) shows the deviation from the fit of the curve. The vertical bars shown were the measurement uncertainties associated with top curve. These uncertainties were due to the presence of noise in the amplifier. The rms deviation of the Casimir force with the theoretical data was predicted as 2.4 pN. This deviation included the corrections due to finite conductivity and surface roughness. This experiment has established the capability of the Casimir force to drive micro and nano actuators.

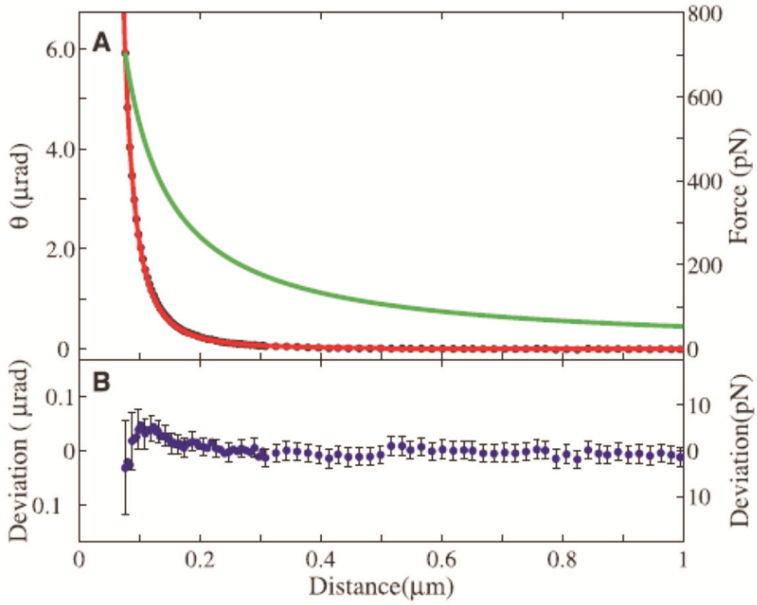

Figure 2.9: (a, top) Red curve represents the fit of the data points obtained through the angle of rotation of the top plate when under the influence of the Casimir force. The green curve represents the electrostatic curve that has the longer range & (b, bottom) Deviation of the measured Casimir force from the theoretical value [6]

The precise measurement of the Casimir force between two metallic plates using micromachined oscillator was measured in three successive experiments performed by *Decca et al.* These experiments did not use the configuration of parallel plates but sphere and plate. The first experiment was made with a Au-coated sphere and Cu coated plate [38-40]. The second experiment with several improvements used both sphere and plate coated with Au [41, 42]. Further improvements implemented in the third experiment with a Au-coated sphere and Au-coated plate made it the most precise and reliable measurement

with metallic test bodies ever performed in the Casimir force measurements to date [43, 44].

In the experiments performed by *R S Decca et al.* [38-44], the Casimir force per unit area (pressure) was measured dynamically by means of a micromechanical torsion oscillator. The oscillator is made of a 500x500 μm^2 heavily doped polysilicon plate suspended along one central planar axis by serpentine springs. A sphere of radius, R=151.3 μm is suspended above it, which is attached to an optical fibre, as shown in Figure 2.10. The experimental setup shown in Figure 2.10 is similar to the one used by *H B Chan et al.*, [6] except that the sphere here was attached to fibre instead of copper wire in [38].

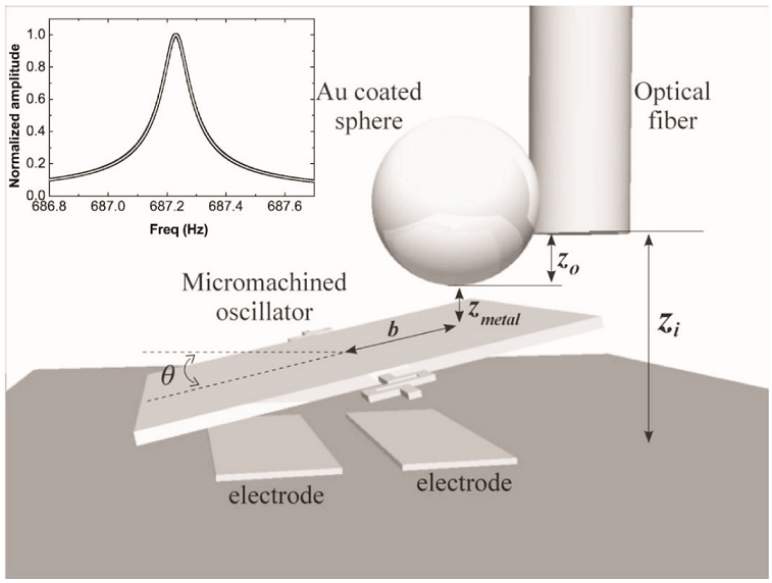

Figure 2.10: Measurement set-up used by Decca et al [38]

The frequency shift $(\omega_r - \omega_0)$ in *Decca's* experiments was directly measured and it leads to the calculated values of the Casimir force gradient $(\delta F/\delta a)$. Using the Proximity Force Approximation (PFA) [21, 22] this gradient can be expressed through the effective Casimir pressure in the configuration of two parallel plates [7, 41]. Here the Casimir force is indirectly measured in terms of frequency shift.

The Casimir pressure calculated from the frequency shift measurements is shown in Figure 2.11. The total relative experimental error varies from 0.19% at separations, a =162 nm to 0.9% at a=400 nm and to 9.0% at the largest separation a=746 nm. Up till now, [43, 44] remain the sole experiment that satisfies one of the main requirement imposed on *precise* experiment in metrology [45].

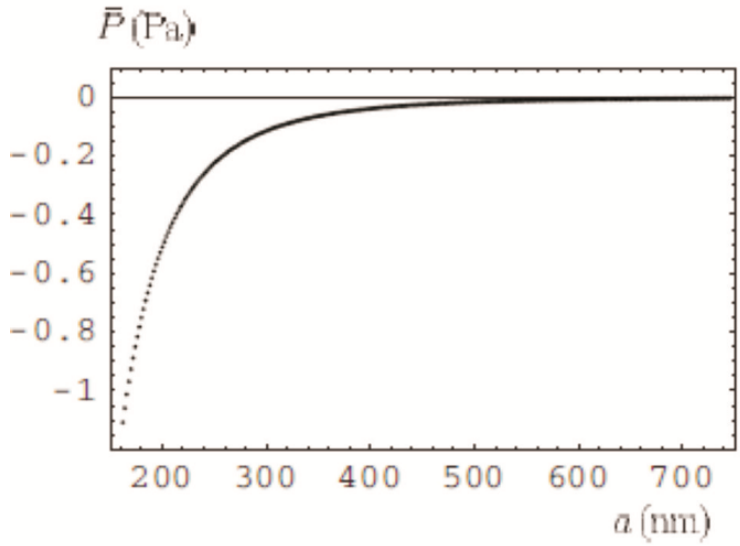

Figure 2.11: Results from [43] showing the mean values of Casimir pressure (dot) Vs separation

2.3.7 Experiments between Parallel Plates - Macro Level Set-up

In the recent experimental investigations, the only experiment which uses the original configuration involving parallel plate geometry was done by *Bressi et al.* [7, 46 and 47]. A cantilever made of silicon and a thick plate rigidly connected to a frame (forms source) both covered with Cr was used for measurement. The separation between the parallel surfaces ranged between 0.5 μm 3 μm. The experimental setup for the Casimir force measurements used by *Bressi et al.* is presented in Figure 2.12.

The separation distance between the cantilever and the rigid plate was first adjusted with a DC motor for large separation and ultimately fine tuning was achieved by using a piezoelectric actuator which was connected to the frame. Actuating the piezoelectric transducer with a sinusoidal voltage produces small oscillations in the rigid plate (source). This in turn induces oscillations of the cantilever through Casimir force. The Casimir force was measured in terms of shift in the frequency of the cantilever. The relative force coefficient was measured with a precision of 15%. The motion of the cantilever beam was monitored by the optical fibre interferometer located opposite side of the resonator. The pressure inside the chamber is maintained at 10^{-5} mbar.

Figure 2.13 shows the Casimir force detection which is a function of residual square

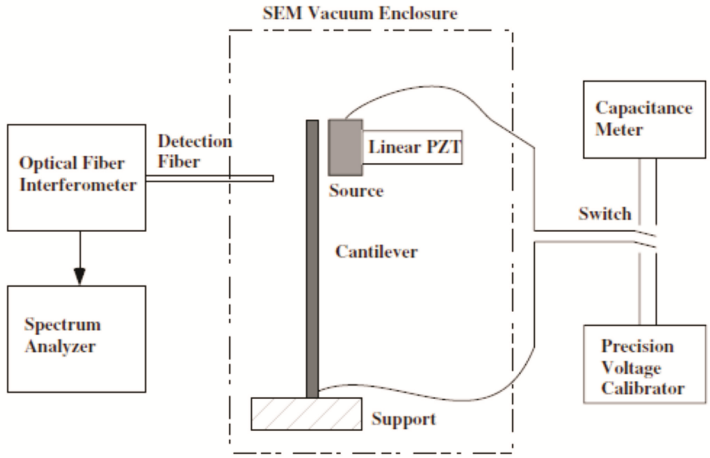

Figure 2.12: Experimental set-up used by Bressi et al. [9]

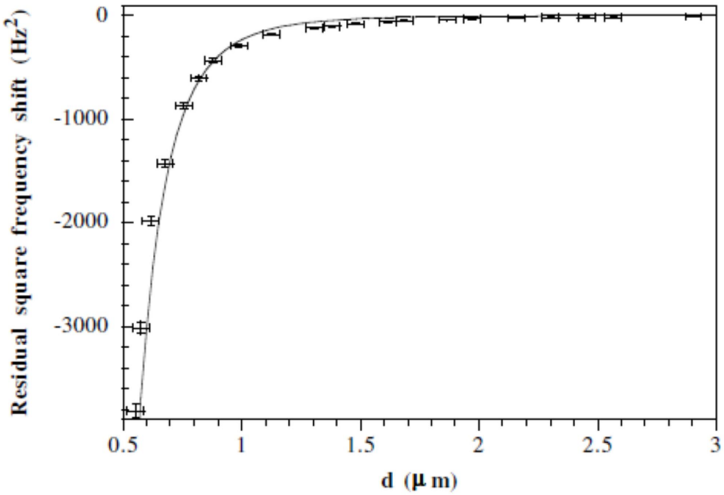

Figure 2.13: Residuals of square frequency shift Vs separation and best fit as observed in Bressi et al experiment [9]

frequency shift of the cantilever beam. The parallel plate configuration as described in this effort provided larger magnitude of Casimir force when compared to the sphere plane configuration. This technique provides a platform for the increased precision of the sensitive Casimir force measurements using the original geometry of parallel plate configuration.

2.3.8 Casimir Force between Dissimilar Media

One of the first experimental attempts to measure Casimir force between dissimilar metals was reported by *Decca et al.* in 2003 [38]. In which they have used Au on sphere and Cu on MEMS torsion actuator. Casimir force measurements were performed for a separation distances ranging from 0.2 μm to 2 μm between the bodies. The results reported within the range of 0.2 μm - 0.5 μm were better than 1% of the theoretical values which includes corrections due to finite conductivity and roughness of the two metals.

Casimir force measurement between dissimilar metals was also reported by *Iannuzzi et al.* [48]. In this experiment by *Iannuzzi et al.*, the Casimir force is measured between a metal boundary and a sphere coated with hydrogen switchable mirrors. The hydrogen switchable mirrors turn from opaque to transparent when hydrogenated. Though the expected outcome was to have weaker Casimir force due to the transparency of one of the boundary, however, no such changes were observed. This counterintuitive phenomenon can be explained by the Lifshitz theory [3]. This shows the effect on the Casimir force due to the optical wavelengths, which are larger than the separation distance.

The skin depth effect on the Casimir force was studied by *Lisanti et al.* [49]. Sphere-plate geometry was used to measure the Casimir force, in which the sphere was coated with metal of different thicknesses. It was observed that when the thickness of the coating is less than the skin-depth of the electromagnetic modes that mostly contribute to the interaction, the force is significantly smaller than that measured with a thick bulk-like film. Such results can help in predicting the influence of Casimir force on micro and nano structures, which are functional in sub-micron distances. With sphere-plate geometry, the Casimir interaction is also modified by changing the carrier density of semiconductor by several orders of magnitude [50].

2.3.9 Measurement of Repulsive Casimir force

The observation of repulsive Casimir force was reported by *Munday et al.* [51]. In which, by choice of suitable materials immersed in fluid, the sign of Casimir force can be changed to repulsive. Dielectric response functions or the material polarizabilities of the interacting materials and the liquid medium play a crucial role in reversing the attractive Casimir force to the repulsive ones. Bromobenzene was chosen as the liquid medium between the gold coated polystyrene sphere and the silica plate because its material polarizability is between the gold coated sphere and silica plate. Figure 2.14 shows the experimental setup used by *Munday et al.* to measure the repulsive Casimir force. Gold coated polystyrene sphere was mounted on the AFM cantilever tip and was lowered towards the bottom flat plate. The entire setup was arranged in the fluid cell filled with Bromobenzene.

The Casimir force measurements were undertaken using the plates made of gold and silica in the same fluid cell setup. The deflection of the cantilever tip was monitored using photo-detector. It is shown in Figure 2.14, that the gold coated sphere and the bottom gold plate show the attractive interactions whereas the similar gold coated sphere has the repulsive interaction with the silica plate. This repulsive nature was observed during the approach and the retraction of the cantilever beam. However, the magnitude of the repulsive Casimir force is smaller than the attractive force. The demonstration of the repulsive Casimir force can pave a way for novel low friction devices. The quantum levitation of the surfaces in the liquid medium is possible which can ultimately reduce the stiction phenomena. The reliability of the NEMS and MEMS structures can be improved by the suitable selection of the optical materials thereby reducing the attractive Casimir force, when they come in sub micron proximity with the adjacent surfaces.

Though various experiments on Casimir force measurement are summarized in previous section, yet many more have been attempted and the number of papers is increasing. Casimir force was also measured in fluidic media; this was performed by *Munday et al.* [52], which received significant controversies [53-55]. This experiment clearly demonstrated the possibilities of engineering the Casimir force in different media. Lateral Casimir effect was demonstrated by *Chen and Mohideen* between a sinusoidally corrugated gold coated plate and sphere [14]. This demonstration may open new opportunities for the use of the Casimir effect for lateral translation in MEMS. Phase change materials that are mainly exploited in optical data storage system are also used to investigate the Casimir force [56, 57]. Between AgInSbTe (AIST) coated surface and a gold coated surface, changes upto 20% at separations of $\sim$100 nm were found (in both experiment

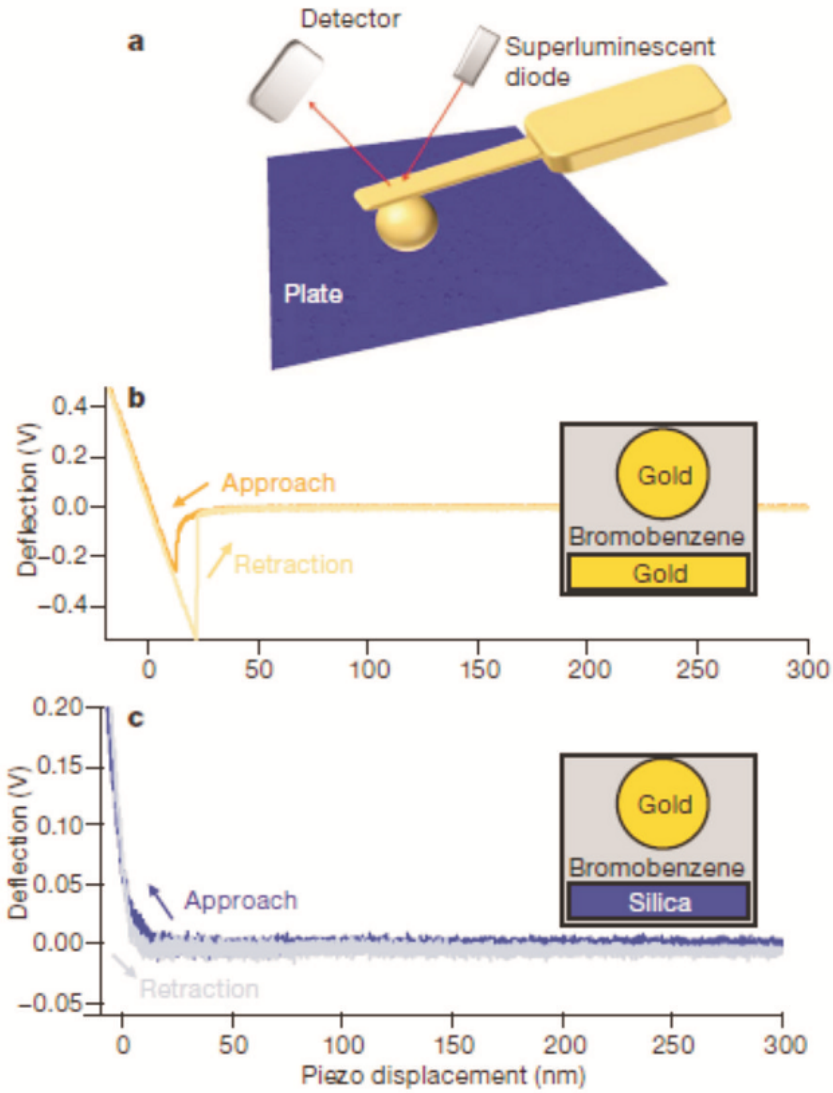

Figure 2.14: Experimental set-up used for measurement, (b) deflection data showing attractive force between the gold sphere and plate & (c) for the same gold sphere and silica plate, deflection data showing the repulsive force [51]

and theory) by changing the AIST from the amorphous to the crystalline phase. Lately, Casimir force measurements using MEMS chip were also investigated [58], in which parallel plate structures separated at $\sim$1 μm distance are realised using MEMS technology.

2.4 Experimental Effort in Current Research

The goal of the current research is to measure the Casimir force using micromachined parallel plate chip, where the plates are separated at sub-micron distance. Exploration of Casimir force in a single chip having dimensions comparable with that of currently used sensors and actuators can provide a new platform that can demonstrate the influence of Casimir force on them. This also allows the use of different material combination which may facilitate to understand the Casimir force.

In the sphere-plate configuration with the use of microsystems, the force is rather weak because of the small effective area of interaction. For macroscopic systems the force can be large, but it is rather challenging to control very small separations. For the plate-plate geometry, one can explore a relatively large interaction area with microsystems increasing the force significantly. However, the precision with which the force can be measured at small separations for example d = 100 - 300 nm, is restricted by 5% due to material dependence [59, 60]. The problem of parallelism which has been an ongoing issue with parallel plate geometry can be solved using methods developed for MEMS design. This geometry is less investigated experimentally and the force between parallel plates can be reliably predicted without the use of additional approximations. Such parallel plate structures can be realised with the advent of micro-fabrication relatively easy. The design principle and the analyses are explained in detail in the following Chapter.

2.5 Summary and Discussions

In this Chapter, Casimir force for the real material properties is presented. A brief history on the prediction of Casimir force is discussed which points out the significant achievements in the electromagnetic field. The Casimir force for real materials as depicted by Lifshitz is also presented. This has been a pioneering work as the original formula derived by H. B. G Casimir was for ideal material properties which could not be directly compared with the measured results. Since the experimental conditions and the real material properties differ from ideal case, the Casimir force for ideal case need to be

modified. These factors which are commonly known as correction factors are also discussed in this Chapter.

An overview of experiments is presented, which briefly explains the major measurement techniques carried out so far. The major requirement in each experiment is the precision with which the measured values are comparable to the theoretical values. This has been significantly improved in recent experiments and is also highlighted in the description. In addition, the essential requirements for a reliable and reproducible measurement of Casimir force are also highlighted.

Most of the experiments carried out so far were with sphere-plate geometry, which required the proximity force approximation to compute the force. Whereas with the parallel plate configuration for which the original Casimir force was derived was seldom used; the prime reason being the difficulty in maintaining parallelism at close separations. The current approach based on micromachined parallel plate geometry is briefly explained here. This approach aims to measure the force within a separation distance of about $\sim$1 μm. In the forthcoming Chapters, the principle of operation, design methodology, fabrication process and the experimental results are described in detail.

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Chapter 3

Casimir Force Measurement: Principle and Design Methodology

Synopsis

In this Chapter[1], the design principle to measure the Casimir force between parallel plates separated at sub-micron distance is presented. The plate-plate geometry was chosen since using MEMS technology it can be fabricated with relative ease. A detailed design analysis of the plate-spring arrangement that ultimately forms the parallel plate geometry is described. An outlook of the possible experimental arrangement to measure the Casimir force with the devised MEMS parallel plate structures is presented and conclusions are drawn.

[1]This chapter is based on the papers published by the author in *Challenges Journal* and *Journal of Micromechanics and Microengineering*. The list of papers by the author is given in Chapter 9.

3.1 Principle of Operation

This section explains the design principle and working of MEMS parallel plate for Casimir force measurement. A schematic overview of the measurement setup is shown in Figure 3.1. The setup consists of two parallel plates, the "actuated" plate and the "responding" plate, measuring a surface area of 1 mm^2. Both plates are coated with a thin layer of gold. The plates are separated by an initial distance d in the order of 1∼2 μm, which is defined by the fabrication process. The plates are fabricated using silicon micromachining and wafer bonding, which is discussed in detail in Chapter 4. The lower, actuated plate is mounted on a piezoelectric actuator (actuating piezo), so that upon actuation it can be moved along the z-axis. The rim of the setup is supported by 3 or 4 additional piezoelec-

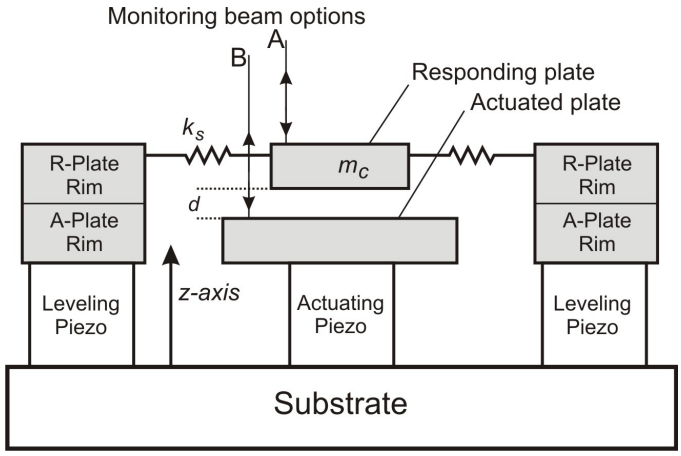

Figure 3.1: Cross sectional view of the measurement set-up. With monitoring beam option A, the responding-plate position is monitored. With option B, the actuated-plate position is monitored. Figure courtesy: T. S. J. Lammerink

tric actuators (levelling piezo), so that the upper, responding plate can be positioned at a well defined distance and exactly in parallel with the lower plate by applying a suitable bias voltages to the actuators. The piezoelectric actuator in the centre is driven by a combination of a DC bias and an AC signal. The DC bias controls the static distance between the parallel plates and the AC signal results in a vibration that modulates the Casimir-Lifshitz (CL) force. An upward movement results in a reduction of the plate separation distance d and thus an increase in force. Therefore, an upward movement of the lower plate due to the central piezoelectric actuator will result in a downward movement of the top plate. Thus, a vibration of the lower plate will result in a movement of the upper plate which is exactly in counter-phase as long as the vibration frequency is kept

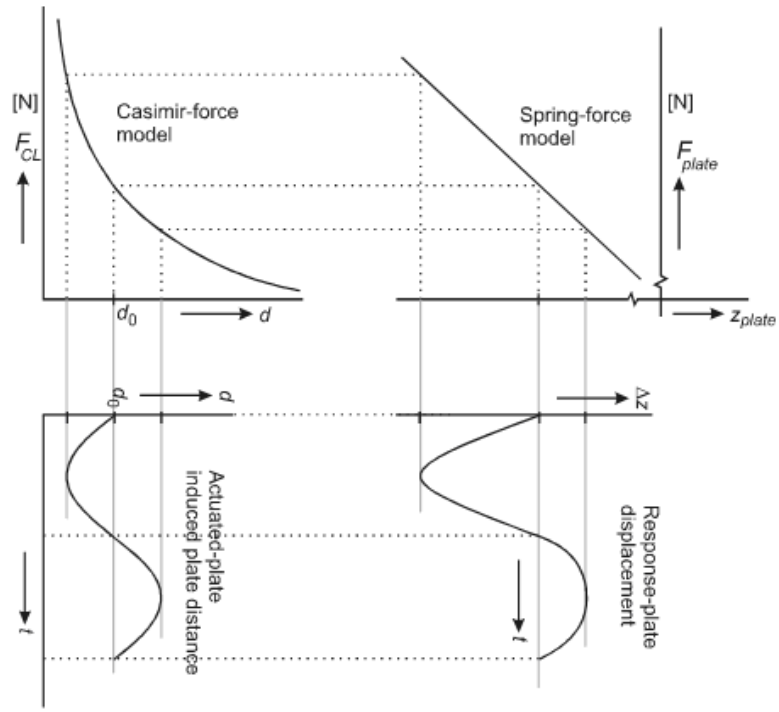

Figure 3.2: Variation of the actuated plate with a harmonic function of time gives rise to variation of the response-plate due to the acting CL force. Note that the response-plate displacement function in the z-direction contains higher order harmonics due to the non-linear characteristic of the CL force with respect to the distance. (F_{el} is assumed to be zero, i.e. the applied potential difference V between the plates is tuned towards a minimum in electrostatic force). Figure courtesy: T. S. J. Lammerink

substantially lower than the resonance frequency of the top plate mass-spring system. To monitor both the plates using a Polytec MSA-400 laser vibrometer, the top plate is designed smaller than the bottom plate. The laser vibrometer also provides the means to monitor the parallelism between the plates, since it can scan the entire top plate and the rim of the actuated plate and thus detect any asymmetry in the vibration modes. At plate separation range of 100 to 300 nm the vibration amplitude of the top plate will be in the order of hundreds of picometers which is substantially larger than the resolution of the vibrometer. The voltages at the levelling piezoelectric actuators are controlled such that the motion of the top plate is a pure up and down motion without tilting of the plate. The setup is operated in vacuum; otherwise the movements of the plates would be strongly coupled by the thin layer of air between the plates. The attainable accuracy will ultimately be limited by the quality of the vacuum, mismatch between the suspension springs, and/or asymmetries of the top plate, and by non-idealities in the actuation piezo's. For example, the central actuation piezo should result in a pure up-down motion of the lower plate, but in practice some bending and tilting of the plate will be inevitable.

Figure 3.2 graphically illustrates the movement of the top plate in response to the actuated movement of the bottom plate. Driving the actuated plate at relatively large amplitudes compared to the average distance, d_0 will result in a non-linear response, as indicated in Figure 3.2. In that case the movement of the response plate contains higher order harmonics that can be used to identify the nonlinear characteristic of the CL force. Alternatively, small actuation amplitudes can be used while measuring the response amplitude as a function of d_0.

3.2 Design Requirements

The design of MEMS parallel plate structures for the Casimir force measurement is based on mass-spring system. Two spring structure design have been considered as presented in Figure 3.3 and are as follows:

- Spring Design1: a simple beam as spring
- Spring Design2: L-shape beam as spring

The top views of the plate with two different spring structures are shown in Figure 3.4. Two types of mass-spring system with different number of springs (4 & 8) connected at the corners of the plate are designed, as shown in Figure 3.5. The choice of the springs is

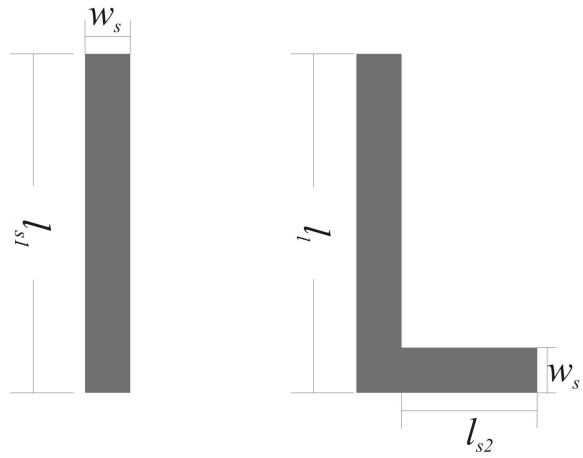

Figure 3.3: Top view of spring structures: (a) simple beam with length l_{s1} and width w_s, (b) L-shape beam with lengths l_{s2}, l_l and width w_s

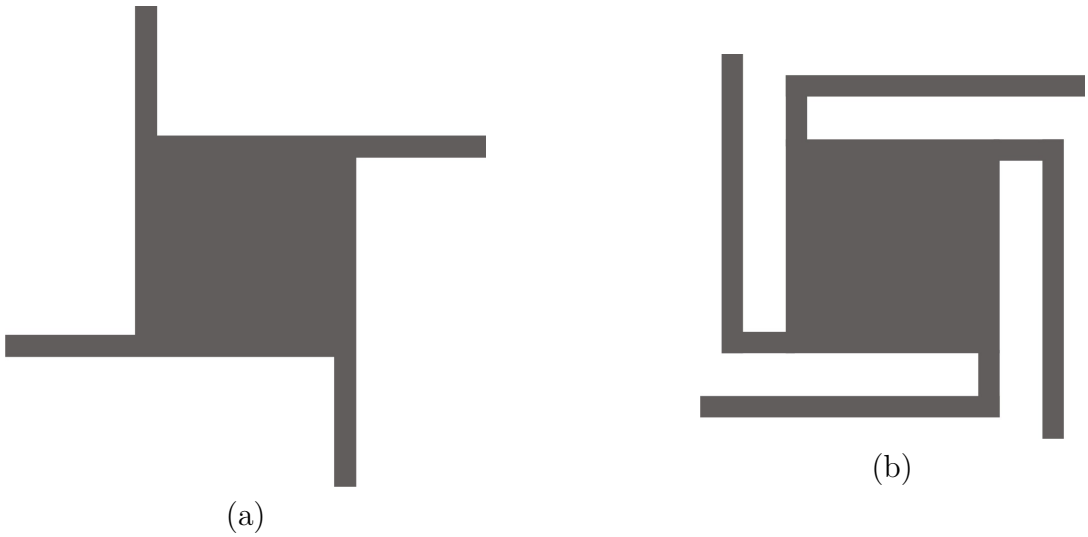

Figure 3.4: Top views of plate with the spring structures: (a) plate-spring design 1 and (b) plate-spring design 2

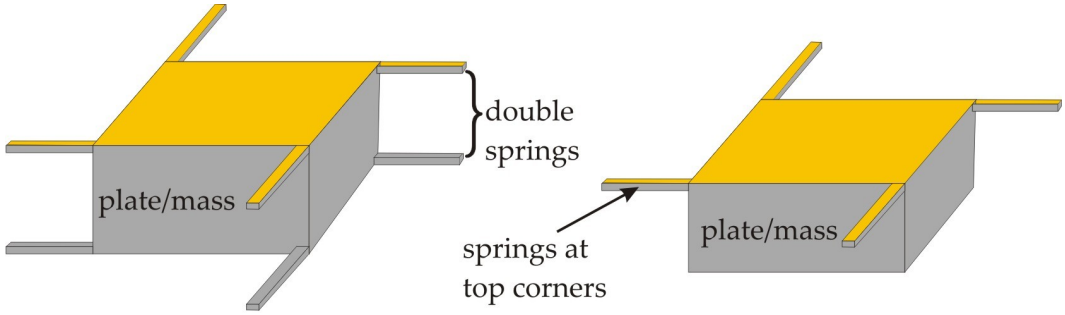

Figure 3.5: 3D image of the spring structure showing the plate with spring(s) at each corner

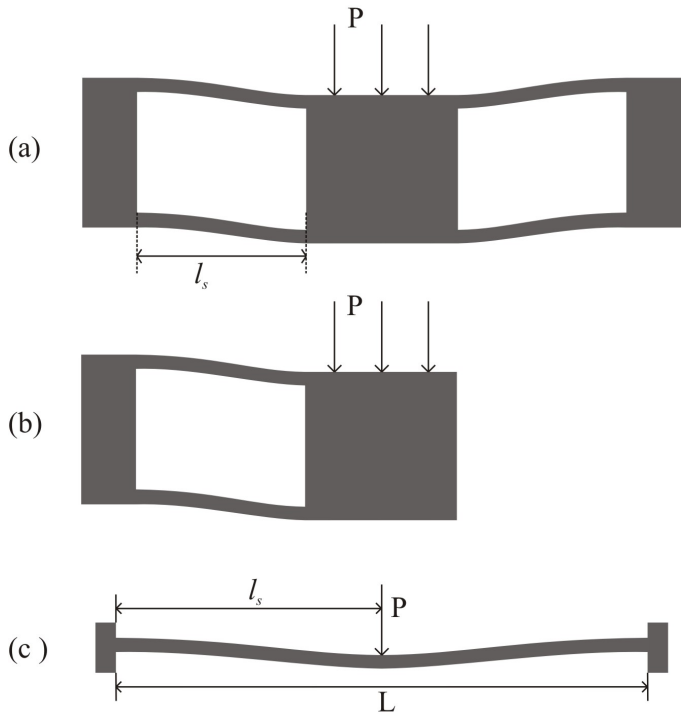

Figure 3.6: Cross Section drawings of the spring configurations (a) & (b) with a distributed load on the rigid plate are assumed to show a deflection equal to a clamped-clamped beam subjected to a centred point load if the total force is the same

motivated as follows: spring design 1 is chosen in order to have relatively rigid structures and spring design 2 has long springs that can enhance sensitivity of the device. The plates with springs at each corner (Fig 3.5(a)) are chosen to be statically indeterminate, whereas the plates with springs at top corners alone (Fig 3.5(b)) are considered to be statically determinate devices. In both the cases, the objective is to keep the plate or mass in parallel position.

3.2.1 Design of mass-spring system

The spring anchored to the frame at one side and connected to the plate-mass at another side is assumed as clamped-clamped beam, as shown in Figure 3.6. It is assumed that the deflection of the rigid plate under a distributed load (spread force) is equal to the deflection of a clamped-clamped beam under a centered point load (concentrated force, equal in magnitude to the spread force). For the calculation of the stiffness (spring constant), the case shown in Figure 3.6(a) is treated equivalent to the case(c). A structure containing N pairs of beam springs each of length l (a total of $2N$ springs), is thought to deflect equivalently to N parallel clamped-clamped beams of length $L = 2l$, For such case, maximum deflection occurs at $x = L/2 = l$, which is given as [1]:

$$\Delta z \left(\frac{L}{2}\right) = \frac{PL^3}{192EI} \tag{3.1}$$

And the stiffness for a rectangular cross-section beam whose length is larger than the width is given as:

$$K_s = \frac{192EI}{L^3} \tag{3.2}$$

where L in both Equations 3.1 and 3.2 is the total length of the beam, in this case it is the length of the spring shown in Figure 3.3. The product EI, is the flexural rigidity, which contains the plate modulus E and the moment of inertia I, for a rectangular cross-section it is given by, $I = wt^3/12$.

In the current case, $L = l$ and the load P is distributed over the spring, hence the Equation 3.2 becomes:

$$K_s = \frac{16EI}{l^3} \tag{3.3}$$

Equatio 3.3 is applicable for the calculation of the stiffness constant of the simple beam spring and small deflection. The stiffness constant for the L-shape beam spring is calculated in the following steps.

Considering the L-shape beam as two long and short beams connected in series, the total stiffness is then given by:

$$K_{tL} = \frac{K_{ls2} \cdot K_l}{K_{ls2} + K_l} \tag{3.4}$$

where $K_{ls2} = 16EI/l_{s2}^3$ and $K_l = 16EI/l_l^3$.

For both spring designs, the total spring stiffness is obtained from Equation 3.5 and is given by:

$$K_{tl} = n \cdot K_s \qquad \text{and} \qquad K_{t2} = n \cdot K_{tL} \tag{3.5}$$

where n is the number of springs connected at the corners of plate. This total spring stiffness (K_{t1} and K_{t2}) is used in the calculation of resonance frequency of both the plates (using $\sqrt{(K_t/m_c)}$).

3.3 Correction Factors

The Casimir force stated in Equation 2.1 is based on ideal mirror properties of material at absolute vacuum and at zero temperature. However, the Casimir-Lifshitz force (CL) measurement experiment discussed in this thesis is measured at finite temperature between the deposited materials that have finite conductivity and roughness. The measured CL force values are comparable with the theoretical values only when the correction factor accounting for the deviation is included in calculation. A detailed account of the correction factors that are essential in real time experiments are described in Section 2.2.2, Chapter 2.

The CL force is often expressed via the pure Casimir force as given Equation 2.1 using the reduction factor $\eta(d)$ [2]:

$$F_{CL}(d) = \eta(d) F_C(d) \tag{3.6}$$

The reduction factor accounts for the deviation of the plate materials from ideal reflectors and for finite temperature. The roughness correction can also be included in the definition of η [3-6]. The reduction factor can be calculated using the Lifshitz theory [7]. As input information in the Lifshitz formula one has to use the dielectric functions $\epsilon(\omega)$ of the interacting materials. The main challenge of using this approach is that the dielectric functions have to be known in a wide frequency range. Special analysis of gold films deposited at different conditions was made by *Svetovoy et al.* [8], where the dielectric functions were measured using ellipsometry wavelengths range of 0.14-33 μm. The reduction factors $\eta(d)$ for these gold films also can be found in [8]. For the measurements

aiming below 2 μm of separation distance, the effect due to temperature can be negligible and therefore has not been taken into account. The reason for this phenomenon has been discussed in Chapter 2 under correction factors Section.

3.4 Mathematical Modelling of Parallel Plate Structure

Design analysis of the MEMS structure to compute the Casimir force has been performed using MathCAD from Mathsoft and Matlab tools [9, 10]. Table 3.1 provides the details of parameters used in the modeling. The spring constant k_s for the suspension springs of the upper, responding plate (see Figure 3.1) has been chosen to be relatively large (in the order of kN/m) since the resonance frequency of the system will impose an upper limit to the actuation frequency of the lower, actuated plate. When the lower plate is driven at a frequency which is substantially lower than the resonance frequency of the responding plate mass-spring system ($\sqrt{k_t/m_c}$) the movement of the responding plate can be considered quasi-static. In order to do that, the resonance frequency is chosen to be $\geq$ 1 KHz, which in turn decides the dimension of the spring structures accordingly. The dimensions of two different springs to obtain relatively large spring stiffness in the order of kN/m are given in Tables 3.2 and 3.3. For top plate dimensions specified in Table 3.1, the calculated resonance frequency is also given in Tables 3.2 and 3.3.

3.5 Design of the Experiments

The vibration amplitude of the top plate is a direct measure for the force between the plates; this force is a combination of the CL force and the electrostatic force acting between the plates due to residual potential difference between plates. The total resulting force can be given as:

$$F_t = F_{CL} + F_{el} \tag{3.7}$$

where F_{CL} is the CL force as in Equation 2.1 and F_{el} is the electrostatic force, which is given by:

$$F_{el} = A\frac{\epsilon_0(V + V_0)^2}{d^2} \tag{3.8}$$

Table 3.1: Parameters used in the modelling of micromachined parallel plates

Parameters	Values
Permittivity of vacuum, ϵ_0	8.854 x 10^{-12} F/m
Planks reduced constant, $\hbar$	1.0510^{-34} Kg m^2 /sec
Speed of light in vacuum, c	3 x 10^8 m/sec
Reduction factor, η	0.5 (for d = 100 nm)
Youngs modulus of Si, E	150 GPa
Density of Si, ρ	2390 Kg/m^3
Poisson ratio of Si, μ	0.27
Lower plate area, A_l	1.1 mm^2
Upper/top plate area, A_t	1 mm^2
Thickness of plate, t_p	380 μm
Interacting area, A	1 mm^2
Initial distance between the plates, d_0	1 μm

Table 3.2: Dimensions of spring design 1 (simple beam spring) and calculated parameters of mass-spring system

Parameters	Values
Length of spring, l_{s1}	800 μm
Width of spring, w_s	50 μm
Thickness of spring, t_s	50 μm
Total spring stiffness, K_{t1}	7.324 kN/m
Mass of plate, m	8.8510^{-7} Kg
Resonance frequency of top plate, fr_{t1}	14.475 kHz

Table 3.3: Dimensions of spring design 2 (L-shape beam spring) and calculated parameters of mass-spring system

Parameters	Values
Length of long beam, l_l	800 μm
Length of short beam, l_{s2}	200 μm
Width of spring, w_s	50 μm
Thickness of spring, t_s	50 μm
Total spring stiffness, K_{t2}	9.6154 kN/m
Mass of plate, m	8.8510^{-7} Kg
Resonance frequency of top plate, fr_{t2}	16.586 kHz

Here ϵ_0 is the permittivity of vacuum, V is the applied external voltage and V_0 is the residual voltage, which inevitably arises due to built-in charges and the presence of different metals in the electrical circuit. The CL force does not depend on the applied potential, therefore, the net force will be minimal when $V = -V_0$. The minimal net force coincides with the CL force, which has been measured. A more sophisticated procedure to determine the electrostatic contribution is described by *De Man et al.* [11] (see also the recent discussion of the electrostatic calibration [11, 12]). A plot showing the total forces and the electrostatic forces acting between the plates for varying DC voltages with varying distance between the plates is shown in Figure 3.7. It is observed that the voltage has to be controlled to less than 1 mV in order for the CL force to be the dominant force.

The force between the plates results in a movement of the top plate towards the bottom plate. For relatively slow changes in time, i.e. well below the resonance frequency of the top plate mass-spring system, quasi static operation can be assumed and the displacement, x_s is given by the following Equation:

$$x_s = \frac{F_t}{K_{eff}} \tag{3.9}$$

where F_t is the total force between the plates as given in Equation 3.7 and K_{eff} is the total spring constant of the 4 or 8 springs connected at the corners of the plate. Equation Equation 3.9 is only valid as long as the resulting displacement is small compared to the movement of the bottom plate, as otherwise the additional reduction of the separation distance due to the top plate movement has to be taken into account.

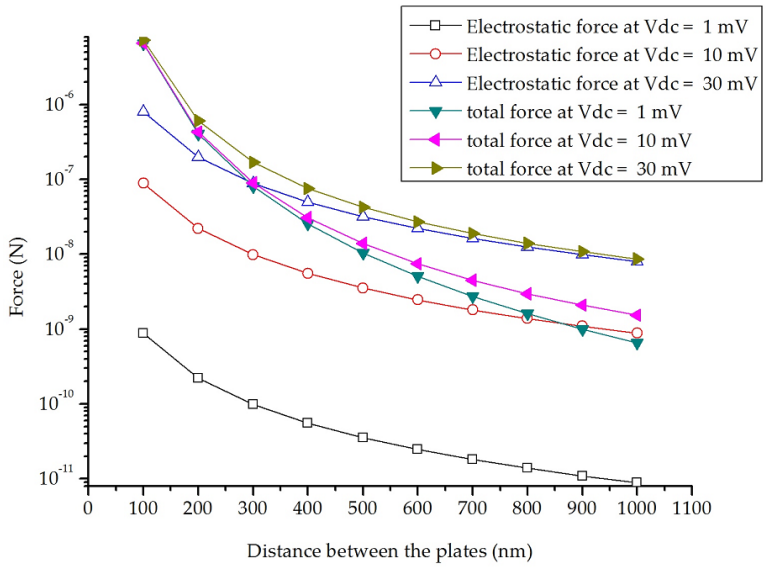

Figure 3.7: Calculated CL and electrostatic forces between the plates for varying separation distance and varying DC bias voltages

3.5.1 Small Signal Actuation for Linear Operation

When the lower plate is actuated by the middle piezoelectric actuator, this results in a variation of the plate distance, d and is given by:

$$d = d_0 - z_{act} \cdot \sin(\omega_{act} t) \tag{3.10}$$

assuming that the resulting movement of the upper plate can be neglected compared to the movement of the actuated plate. Here, d_0 is the average distance between the plates, Z_{act} the actuation amplitude and ω_{act} the actuation angular frequency. The change in CL force and the associated movement of the upper plate due to this variation in distance can be calculated using Equations 3.7 and 3.9. As mentioned before, the actuation frequency ω_{act} should be well below the resonance frequency of the top plate mass-spring system so that the movement can be considered quasi-static.

In addition to an AC signal to drive the actuator, a DC bias voltage can also be applied. In this way, the average distance d_0 between the plates can be decreased, which results in an increased vibration amplitude of the top plate due to the larger CL force. Figure 3.8 presents the calculated vibration amplitude of the top plate as a function of the average distance, d_0 for three different AC actuation amplitudes Z_{act} such as 10nm,

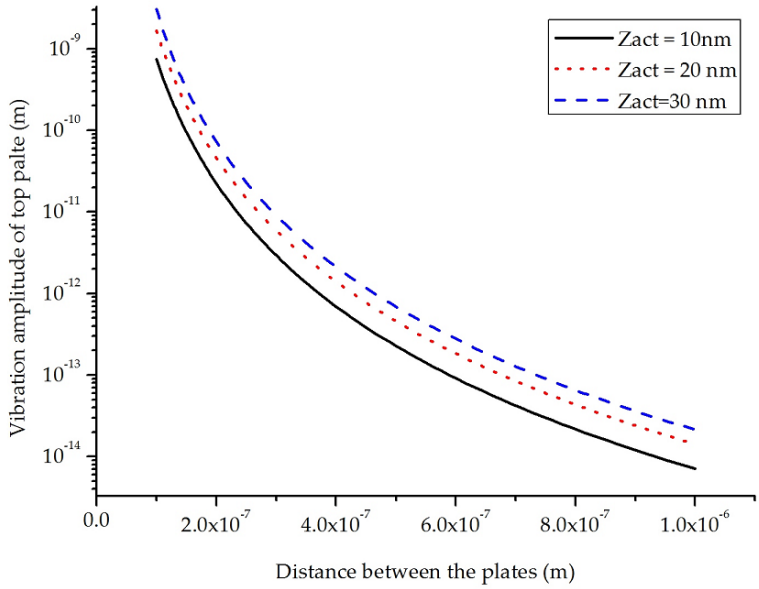

Figure 3.8: Calculated vibration amplitude of upper plate as a function of the average distance d_0 for three different AC actuation amplitudes (axes are in logarithmic scale)

20nm and 30nm. From Figure 3.8, it is observed that the movement of the top plate is indeed much smaller than Z_{act} so that the additional reduction of the plate distance due to the movement of the plate can be neglected. It can also be observed that for separation distances above 500 nm, the top plate movement becomes extremely small and difficult to detect.

3.5.2 Nonlinear Behaviour and Higher Harmonics

To increase the movement of the top plate, larger actuation amplitude of the bottom plate can be used. However, in that case the top plate movement will no longer be proportional to the bottom plate movement, resulting in the non-linear response as indicated in Figure 3.2. In this case, Equations 3.7, 3.9 and 3.10 can still be used to calculate the instantaneous displacement of the top plate as a function of the bottom plate position. Using a sinusoidal actuation signal, the resulting top plate movement as a function of time can be calculated. Fourier transform can be used to evaluate the amplitudes of the 1^{st} and higher harmonics of the top plate vibration. Figure 3.9 shows the calculated 1^{st} harmonic as a function of separation distance for several actuation amplitudes and Figure 3.10 shows the higher harmonics.

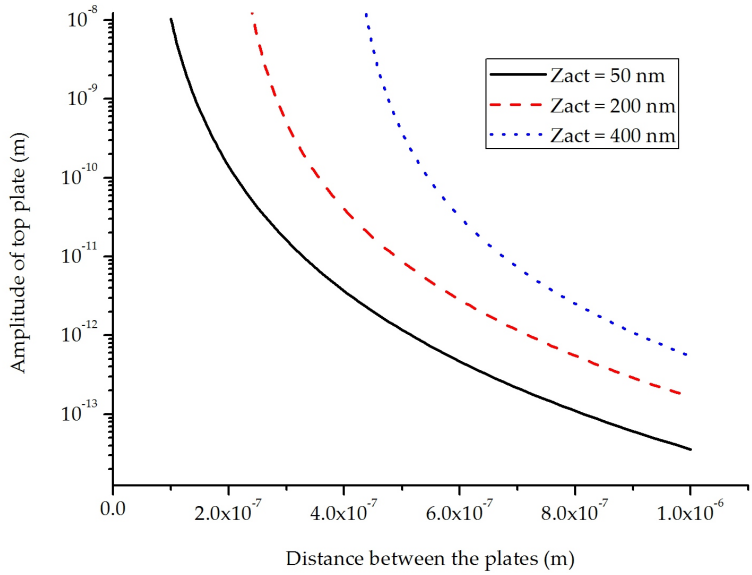

Figure 3.9: First harmonics of top plate movement for different actuation amplitudes (axes are in logarithmic scale)

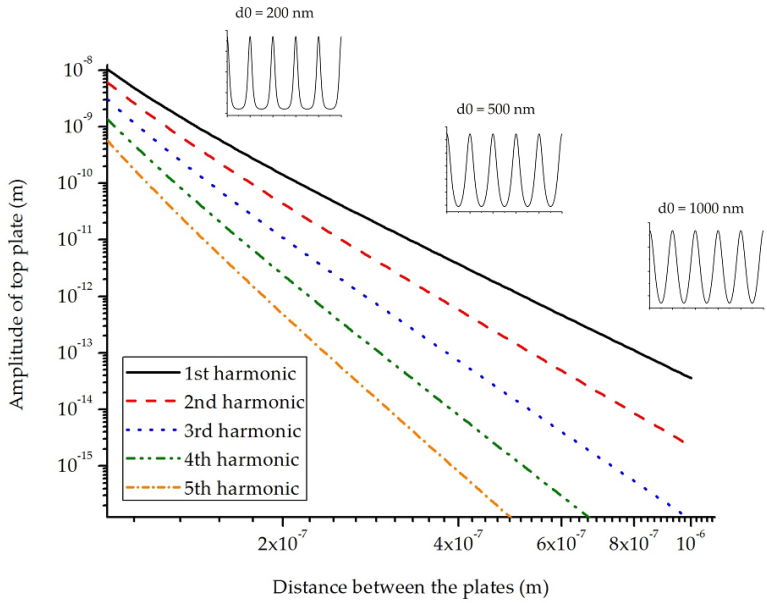

Figure 3.10: Harmonics of top plate movement for an actuation amplitude of 100 nm and an applied DC bias of 30 mV (axes are in logarithmic scale)

3.6 Conclusions

This chapter discussed in detail the design principle and analysis of parallel plate structure for Casimir force measurement. The plate-spring structures were designed based on the principle and scope of the measurement set-up presented here. Different measurement schemes are presented that can be applied to measure the Casimir force in terms of top plate displacement. The calculated results presented here will be used as reference to compare the measured results. The experimental verification of the Casimir force measurements presented here is studied in Chapter 5.

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Chapter 4

Casimir Force Measurement: Fabrication of Parallel Plate Structures

Synopsis

Two possible approaches based on two different substrates to fabricate the parallel plate structures separated at sub-micron distance are discussed in this Chapter. Section 4.1 gives the general requirements that remain the objective of the fabrication processes. Both the fabrication processes are described in Section 4.2 and 4.3. Subsequently, the fabrication results and in depth details of the critical steps that are observed during the fabrication process are presented in Section 4.4. The bonding and chip assembly procedures are briefly discussed in Section 4.5. A qualitative comparison of both the processes has been summarised.

4.1 General Requirements

Casimir force theory was formulated under ideal conditions such as plane parallel geometry with perfectly flat surfaces and perfect reflection. It is a challenge to realize a practical setup to mimic these conditions. In most of the experimental studies, an important factor that increases the measured Casimir Lifshitz (CL) force with respect to the theoretical prediction is the surface roughness of the interacting bodies as discussed in [1-3]. As the surfaces of the real bodies after deposition of gold becomes rougher, it is essential to have a low surface roughness for the plates before depositing the gold layer. Upon deposition of gold, the ultimate roughness will then be the roughness of the gold layer alone.

Considering these facts, the fabrication approach is focused on obtaining optimally flat surfaces. Bulk micromachining is preferred over surface micromachining, as a thick mass is favourable because a thin surface micromachined mass would bend due to the deposited gold layer at a later stage. The fabrication of plates and the suspension springs using single crystal silicon micromachining offers also a mono-crystalline suspension, and minimizes hysteresis and creep. As described in the previous Chapter, two types of plates with spring structures are devised to make the parallel plate structures. Figure 4.1 shows the 3D drawing of two different plate-spring structures and the cross sectional drawing of bonded top and bottom plates.

Two possibilities to realise the envisioned structure are devised. The first process is based on <111>-oriented silicon substrates, which have shown to yield beams and plates with smooth surfaces when processed with a combination of Deep Reactive Ion Etching (DRIE) and wet anisotropic etching [4]. The second scheme is using Silicon On Insulator (SOI) wafers. In both the fabrication processes, the main requirement is to have bonded plates separated at a distance of $\sim$1 μm. To accomplish this, two types of bonding techniques are explored that are feasible with the respective process schemes. One of the methods is based on direct Silicon-Silicon (Si-Si) bonding for <111> substrate process, and the other is using eutectic bonding of Gold-Silicon (Au-Si) alloy for SOI substrate. Both the fabrication schemes are explained in detail in the forthcoming sections.

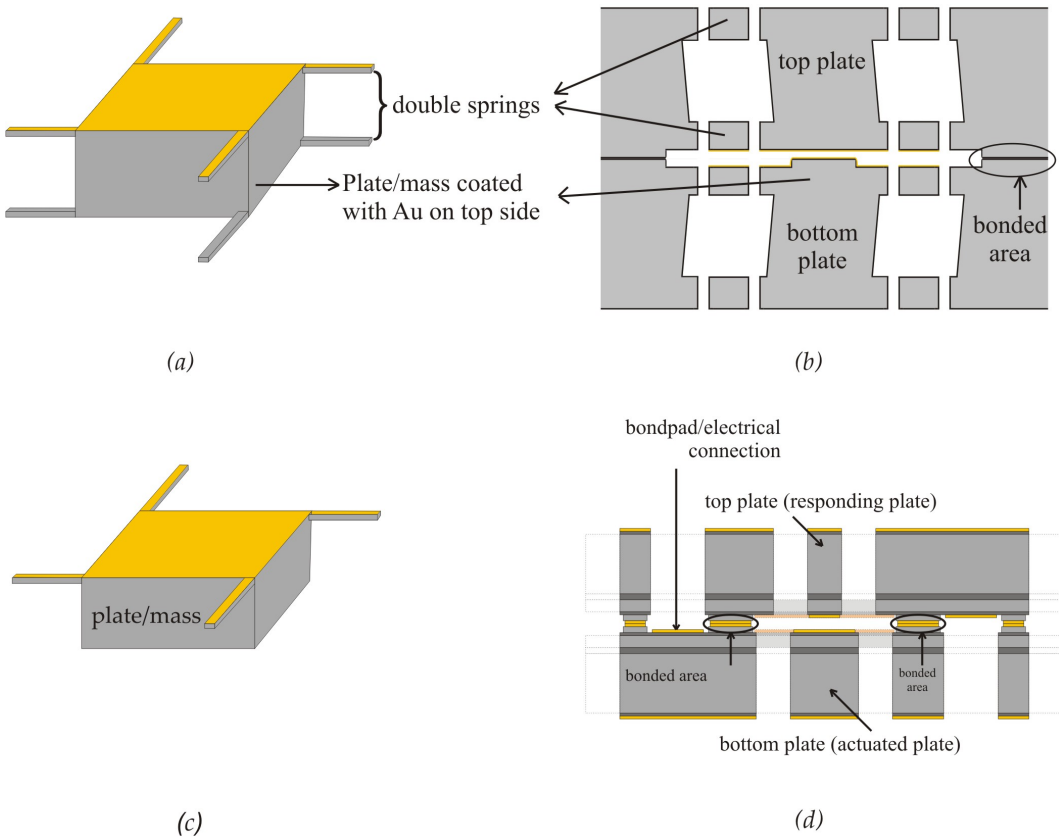


Figure 4.1: (a) 3D view of plate with springs at each corner of the plate, in total with 8 springs (Design 1), (b) Cross sectional view of the bonded plates with the separation distance, d being defined by an elevated bump on the lower plate of the structure. (c) 3D view of plate with springs at each top corners of the plate, in total with 4 springs (Design 2), (d) Cross sectional view of bonded top and bottom plates with the separation distance, d being defined by the spacers at the bonded area.

4.2 Fabrication Process Based on <111>-Oriented Substrates

Unlike <100> or <110> wafers, the surface parallel to the <111>-orientation gives better surfaces with roughness equivalent to atomically flat surfaces [4-6]. As mentioned before, this fabrication process is devised to obtain plates with smooth surfaces which are one of the main requirements for the Casimir force measurement. The smooth surfaces also facilitate the direct bonding of two similar wafers. The design is made in such a way that both top and bottom plates are processed in one substrate and ultimately bonding two similar substrates result in parallel plates separated at $\sim$1 μm distance. This process scheme is developed to realise the parallel plate structure having 8 springs at each corner as shown in Figure 4.1 (a) and (b). The process outline is shown in Figures 4.2 and 4.3, which shows the cross section of the bottom plate with an elevated area at its centre.

The process starts with the formation of shallow cavities. In order to obtain good uniformity and low surface roughness, this is performed by local oxidation of silicon followed by removal of the oxide [7]. In Figure 4.2, first, a layer of 100 nm thick Silicon Rich silicon Nitride (SiRN) is deposited on both sides (step1), followed by a 50 nm thick polysilicon layer (step 2). The polysilicon is shortly oxidised to form a thin layer of oxide, about 20 nm (step 3). This oxide layer is used as etch mask when patterning the polysilicon in wet chemical etchant (25% TMAH). The oxide is then patterned with a positive resist and is etched in 1% HF followed by the removal of resist in acetone. Subsequently, polysilicon is etched in 25% TMAH. With polysilicon as mask, the SiRN is then etched in 50% HF (step 4). After etching SiRN, the unmasked silicon areas are oxidised using wet oxidation at 1000^oC (step 5).

Following the oxidation, both the oxide and nitride layers are removed in 50% HF, which results in pure silicon patterned with shallow cavities measuring a depth of $\sim$1 μm (step 6). The depth of these cavities depends on the oxidation depth of the silicon. Therefore, to get a cavity of $\sim$1 μm, prolonged oxidation is required to get a thick layer. Wet oxidation is preferred over dry, since the observed oxidation rate was significantly higher. The absolute depth of the formed cavities is measured with a surface profilometer after removing both the oxide and nitride layers.

The process continues by patterning the plates and springs, from step 7 as shown in Figure 4.3 (a). First a 100 nm thick SiRN layer is deposited both sides, followed by a very thick layer of Tetra Ethyl Ortho Silicate (TEOS) oxide, $\sim$1700 nm, refer step 7. These

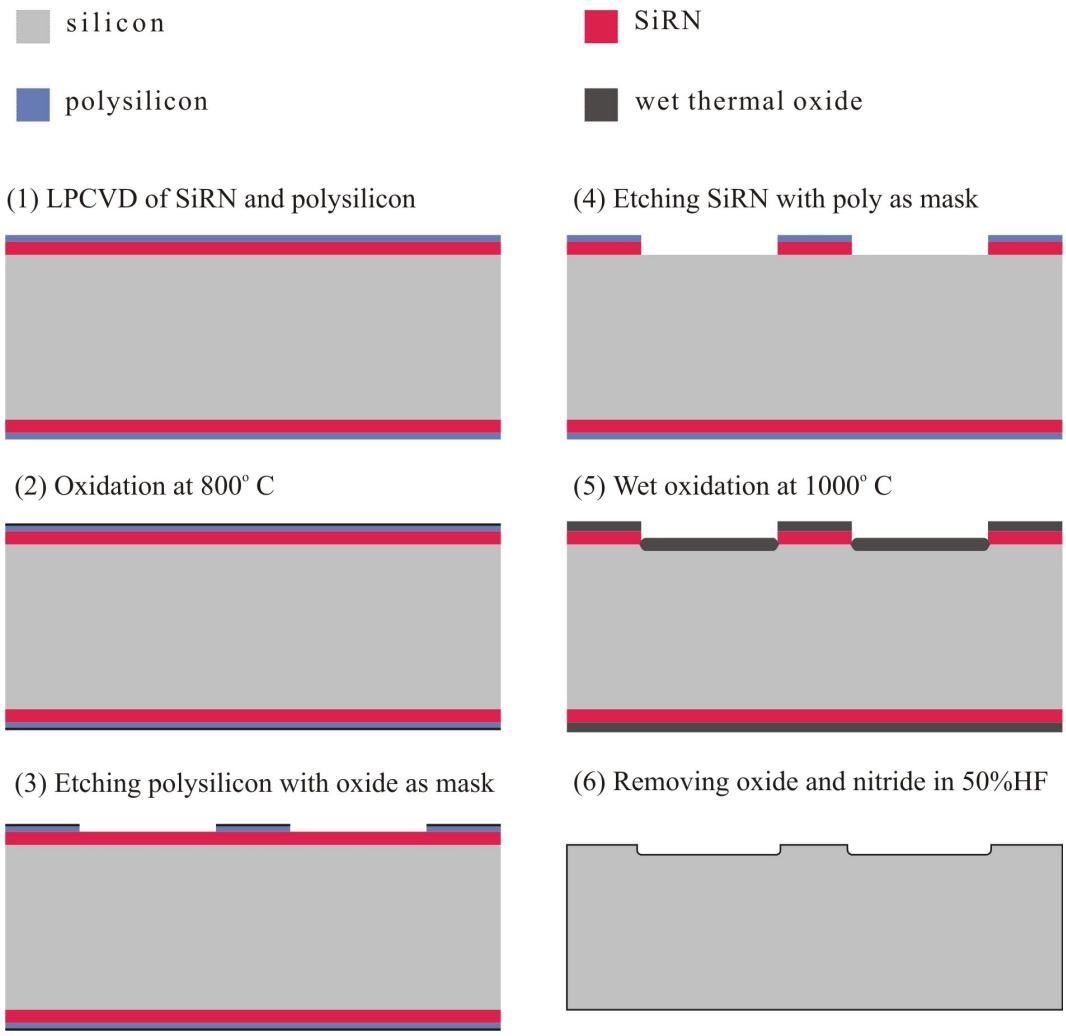


Figure 4.2: Fabrication process outline to create shallow cavities in silicon substrate based on <111> orientation

layers will act as masking materials during DRIE of silicon, in step 12. The etching of TEOS, SiRN and silicon is performed with the same mask material. To accomplish this, SU-8 photoresist is used, which offers a wide range of thickness from <2 μm to >500 μm. Further, it is also well known for its vertical sidewall profile and high aspect ratio [8-9]. The vertical sidewall profile is essential for protection of the corners of the structure during directional etching.

Since the plate-spring structure shown in Figure 4.1 (a) is modelled in a symmetrical design; the backside of the wafer is also processed for patterning of SiRN, TEOS and silicon, see step 9 in Figure 4.3 (a). After removing SU-8 in "piranha" solution (H_2SO_4:H_2O_2, 3:1), SiRN is etched for a short time (∼100 nm) in hot phosphoric acid (H_3PO_4) to expose the silicon at the corners of the springs and plates. Later, these corners of springs and plates are protected by layers of wet oxide and TEOS, see step 11. The reasons for the short etching of SiRN in H_3PO_4 and the two types of oxide requirement are explained later in this section.

Subsequently the oxide at the bottom of the cavities is removed by directional etching and is sequenced with the directional etching of silicon from both sides using DRIE. During this DRIE, a special carrier wafer is used. This carrier wafer is mounted beneath the device wafer and Fomblin oil is used for thermal contact between these two wafers. The reason for this approach is to keep the helium (He) backside cooling system functional throughout the etching of silicon through the wafer using DRIE. When there are holes present in the wafer during this etching of silicon through the wafer, He starts leaking into the etching chamber and the cooling is not functional anymore.

The carrier wafer used in step 12 is patterned with cavities and channels forming a drainage system. These cavities and channels help to prevent the devices from being damaged. This could happen when there is a pressure difference present over a small silicon membrane, which will ultimately damage the membrane if the difference becomes larger. After DRIE (step 12), the silicon is etched in wet anisotropic etchant (25% TMAH at 70^o C) to release the springs (step 13). Prior to gold deposition, all previously deposited layers of nitride and TEOS (in steps 7 and 11) are removed in 50% HF (step 14). After that, the silicon is oxidised to get a thin layer of SiO_2 with a thickness of about 10-20 nm to prevent formation of a eutectic gold-silicon alloy (step 15). A 100 nm gold layer is locally sputter deposited using a shadow mask. Finally, the parallel plate structures separated at ∼1 μm distance is realized by direct bonding of two similar wafers facing their smooth surface areas together in a clean environment at room temperature. The

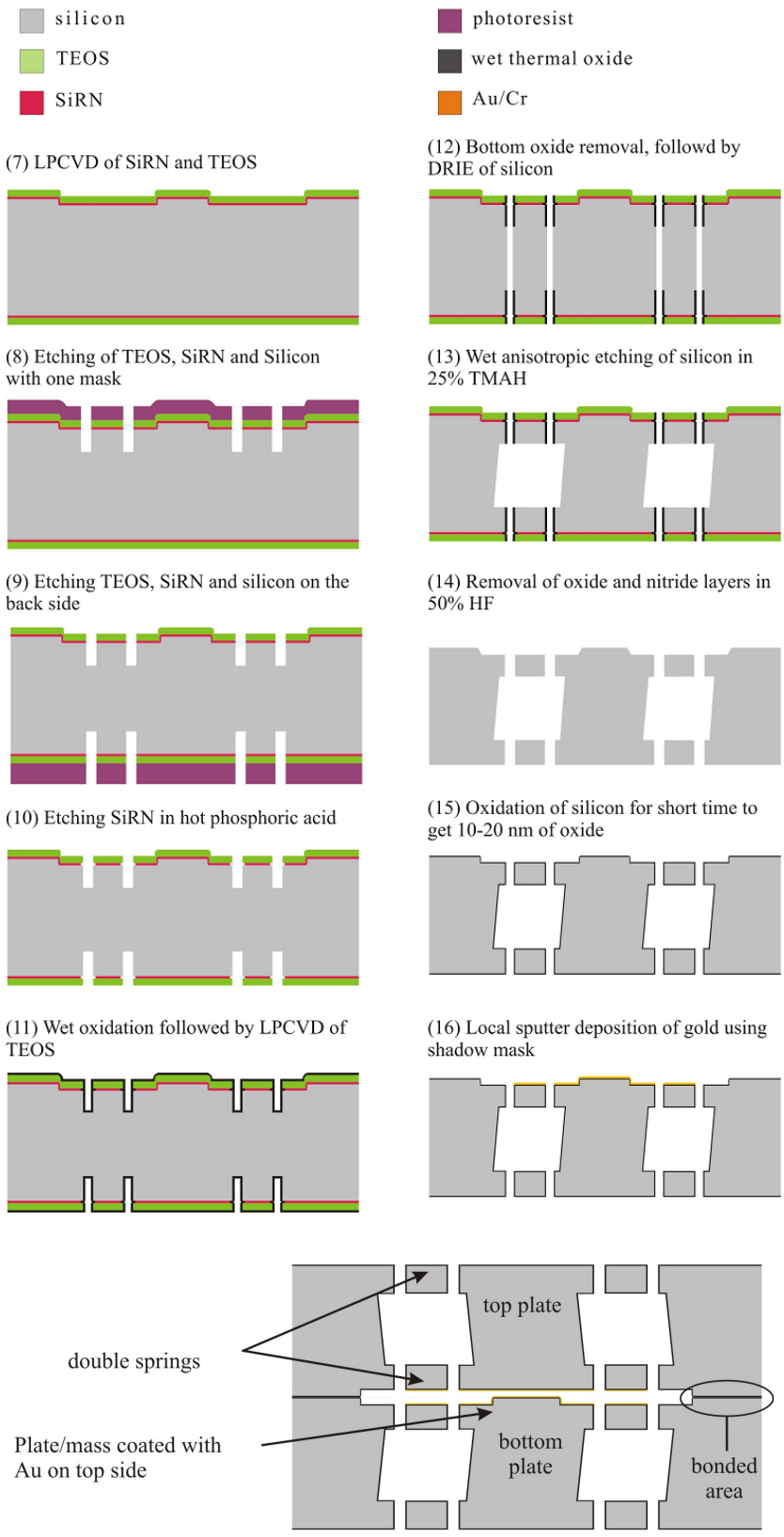


Figure 4.3: Outline of fabrication process (a, top) & cross section of bonded plates (b, bottom)

substrate is then broken apart at the breaking grooves (these are etched during steps 9 & 12), to separate the parallel plate chips. Figure 4.3 (b) shows a cross-sectional drawing of bonded top and bottom plates. All the process parameters including shadow mask wafer and carrier wafer are given in Appendix A.

4.2.1 Bird's Beak Profile and Conformal Layer

Both the wet oxide and TEOS layers act as the sidewall protection for the springs and plates during DRIE through the wafer and wet anisotropic etching of silicon that follows (steps 12 & 13). The width and thickness of the springs is defined by the SU-8 lithography and etched depth of the silicon, however, the cross section is defined by the anisotropic wet etching in step 13 that releases the spring structures. To protect the spring structures during the anisotropic etching, a material that can resist the wet etchant and as well protect these springs is needed. A combination of wet oxide and TEOS oxide is chosen for this purpose. To lay the layers of wet oxide and TEOS oxide, SiRN is etched for a short time (to etch away ∼100 nm of SiRN) so that the corners of the springs are exposed, and are oxidised shortly to get a thin layer of silicon dioxide (50 nm). This helps to create the bird's beak profile at the interface of SiRN and the silicon by oxidising the silicon underneath as shown in Figure 4.4. The bird's beak profile results due to the possibility of oxidant diffusion and thereby allowing lateral oxidation of the silicon underneath the SiRN [10].

Though its presence is regarded as drawback in Complimentary Metal Oxide Semiconductor (CMOS) industry, in the present case it helps in providing additional protection for the corners of the springs from being attacked by the TMAH etchant during spring release etching. The conformal layer of TEOS in addition to the wet oxide in step 11 adds to the top layer thickness of TEOS. When the bottom oxide is etched in step 12 prior to DRIE of silicon, similar thickness of oxide (TEOS in this case) is also etched from top surface. This will considerably reduce the overall thickness of TEOS at the top surface. Therefore, with the second TEOS layer, the top layer thickness of TEOS still remains sufficient to protect the top surface of the springs and plates during through wafer DRIE.

4.3 Fabrication Process Based on SOI Wafers

The fabrication process using SOI wafers is mainly developed with the conception of easy fabrication and to have a reliable and strong bonding of plates to obtain separation

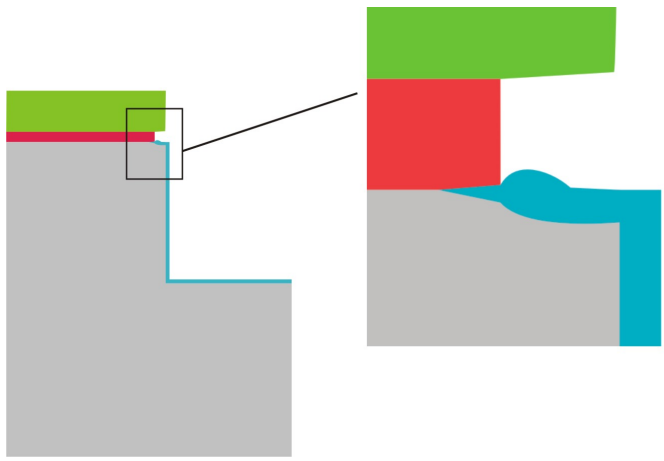
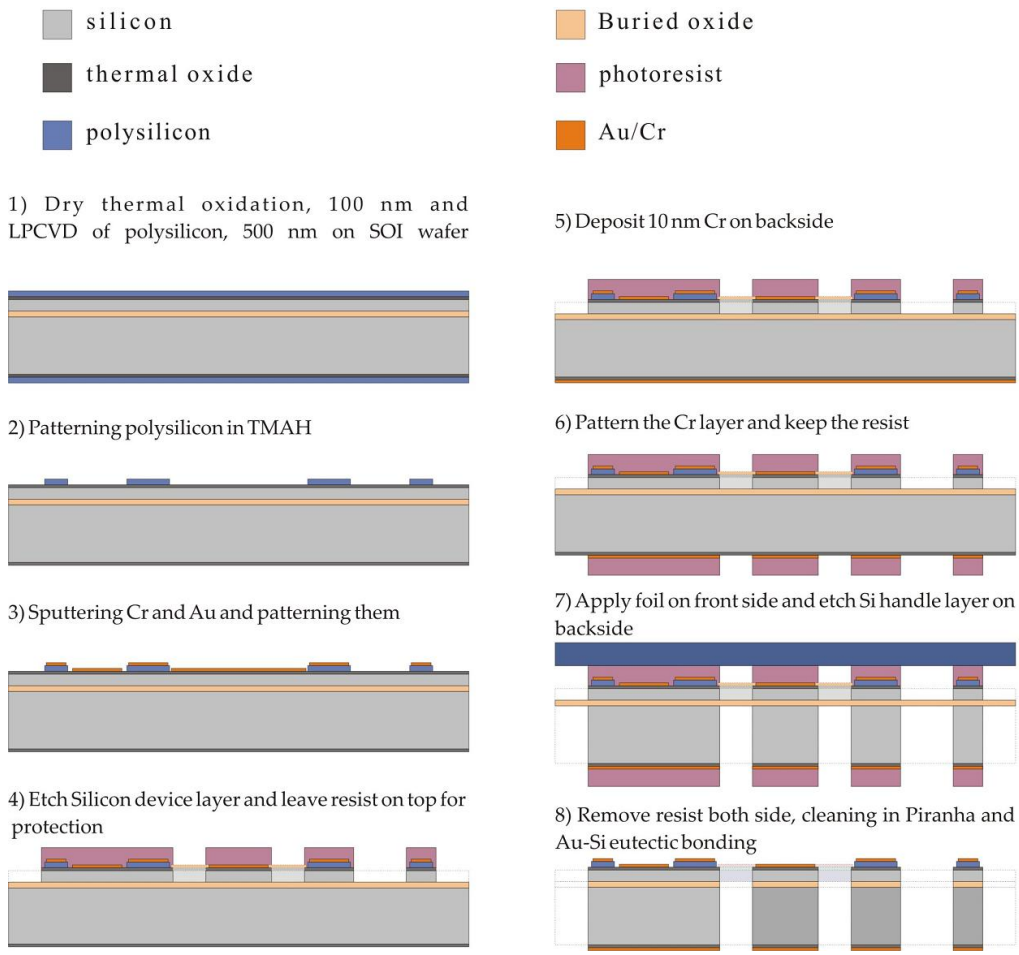


Figure 4.4: Spring sidewall cross-section showing the bird's beak effect.

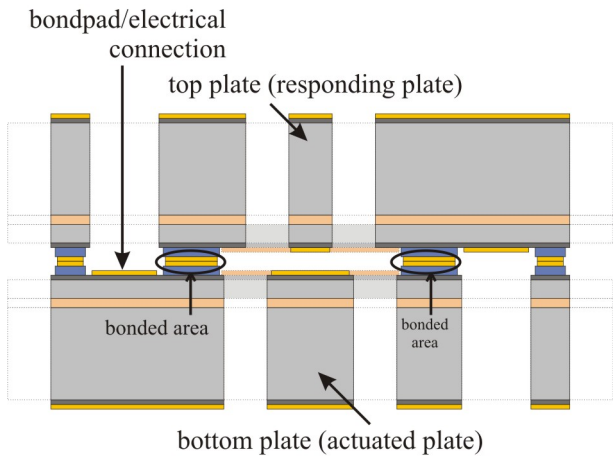
distance in the order of 1 μm. With this approach, the plate structure having 4 springs at top corners of the plate as shown in Figure 4.1 (c) and (d) (design 2) is aimed to be realised. The process starts with SOI wafers having a device layer of 50 μm, buried oxide (BOX) of 1 μm and 380 μm thick handle layer. Since the design 2 consisted of springs at only one side of the plate, the processing steps are reduced compared to the previous scheme.

Though this process is comparatively more promising in terms of yield and reproducibility; however, it has to be compensated with the reduced mechanical stability of the devices due to one sided springs. This process does not give the extremely flat <111> surfaces for the plate structures. However, limited surface roughness is maintained as small as possible during the whole processing. Besides, an alternate bonding process using eutectic silicon-metal alloy is developed that resulted in a strong bond between the plates with defined small separation distance.

The complete process is shown in Figure 4.5. With this process too, the design is made in such a way that when two processed wafers are bonded together, the complete parallel plate chip is formed as shown in Figure 4.1 (d). The bonding used here is metal-silicon eutectic bonding, for which a combination of gold layer and polysilicon has been used. As in the previous process the main requirement with this process is also to have an as smooth as possible surface for the plate structures. Therefore, due care must be given to minimize the increase of the initial surface roughness during further processing. The process starts with creating the spacing layer that defines the initial separation distance between the bonded plates. To realise this, 100-150 nm thermal oxide is formed, followed



(a)



(b)

Figure 4.5: (a, top) Outline of the fabrication process based on SOI substrates & (b, bottom) Cross section of bonded plates

by the deposition of a layer of 500 nm thick polysilicon, step 1, in Figure 4.5. The thermal oxide acts as an isolation layer between the device layer silicon and the polysilicon layer. To get a separation of 1 μm $\pm$100 nm between the bonded plates, the tolerance on the thickness of the polysilicon layer should be within 5 %.

After patterning the polysilicon layer, a 100 nm thick gold layer is deposited with 10 nm chromium (Cr) as adhesion layer (step 3). The resist is removed and lithography with a new mask defining the plate-spring connected to the solid frame of silicon is performed. The chip break lines are also defined in this mask which is etched together with the patterning of the silicon device layer, as in step 4. By keeping the resist on the top side as protective layer, a thin layer of Cr is sputter deposited on the backside, as shown in step 5. This metallic layer at the back side of the wafer is necessary to have a good reflection during measurements which is done using Laser vibrometer.

To release the springs, the back side layers of oxide, handle layer and the BOX layer are etched using DRIE. To keep the backside helium cooling functional and also to protect the devices, the front side of the wafer is covered with a foil (DuPont Mx5000). A 3.5 μm thick layer of photoresist is used as mask material to withstand the long DRIE run to etch through all the layers. After etching the silicon through the wafer, the photoresist is removed and wafers are cleaned in Piranha solution and are ready for Au-Si bonding. The process parameters of this fabrication scheme are given in Appendix B.

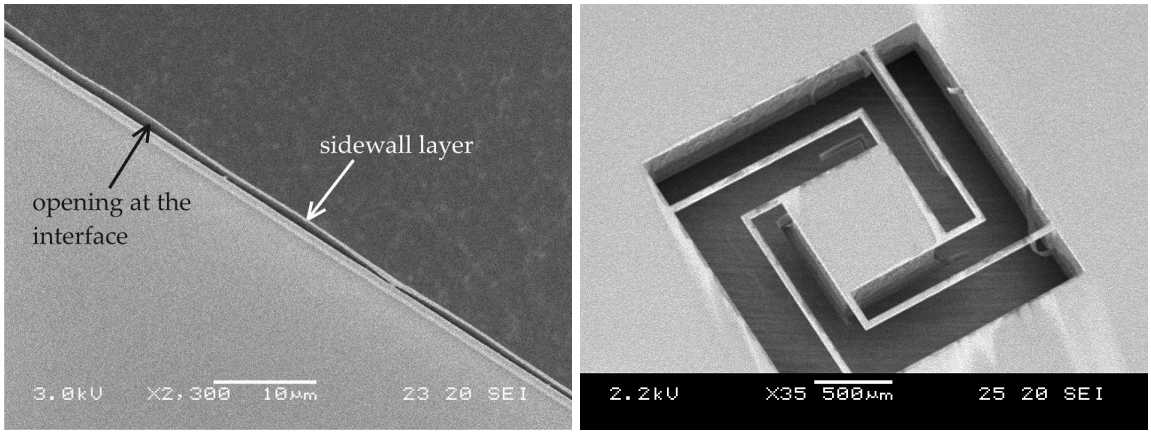
4.4 Results and Discussion of Fabrication Processes

The fabrication schemes described in the previous sections are initially tested with test structure fabrication and then the fabrication of real devices is carried out. The test runs were performed to check the critical steps in the processes. With the initial test runs, the fabrication process devised with <111>-oriented silicon substrate resulted in smooth surfaces with a roughness in the order of $\sim$3 nm. However, during the subsequent process run to realise the parallel plate structures, it was observed that the fabrication process is critical at certain steps that needed additional optimisation. Whereas, the process based on SOI substrates resulted in successful realisation of parallel plate structures separated at $\sim$1 μm distance, though with this process too, there were some critical steps, which need additional optimisation. Further, this fabrication process appeared as a reproducible and reliable scheme to realise parallel plate structures separated at $\sim$1 μm distance. In

the following sections, the results and critical steps of both the fabrication processes are discussed.

4.4.1 Results and Discussion of <111> Fabrication Process

During etching through the wafer (Step 12, Figure 4.3 (a)), it was observed that the edges of the TEOS mask layer did not survive long enough to fully protect the corners of the springs and plates. As a result, a narrow trench is etched between the sidewall protection layers and the silicon, as shown in Figure 4.6 (a). During the subsequent anisotropic wet etching step this resulted in severe etching of the silicon within the sidewall protection layer, as shown in Figure 4.6 (b). As a result, the fabrication process had to be slightly modified. To avoid the undesired etching of silicon within the sidewall coating, a thick mask material that can protect the corners and sidewall during the long wafer through DRIE (Step 12 in Figure 4.3 (a)) is desired. SU-8 100 with a thickness of about 100-150 μm has been used, which completely fills the openings created in step 11. A detailed representation of using SU-8 to fill the cavities and as well to protect the sidewall of springs and plates is shown in Figure 4.7.



(a) (b)

Figure 4.6: (a) Top view showing the opening separating the sidewall protection and silicon during wafer through DRIE. (b) Resulting severe damage to (especially the bottom) suspension springs during subsequent wet anisotropic etching of silicon.

In the process outline shown in Figure 4.3 (a), after the process step 11, using an additional lithography with SU-8 100, openings are created inside the already etched cavities. Subsequently, the removal of bottom oxide and DRIE of silicon is performed

as in step 12. In this case, both the corners and sidewall layers of the springs are well protected and the very thick layer of SU-8 makes it possible to etch longer and deeper. To etch through the whole wafer, etching was done from both sides, and therefore SU-8 is removed from the front side after etching half way through and lithography and similar etching processes are carried out on the other side.

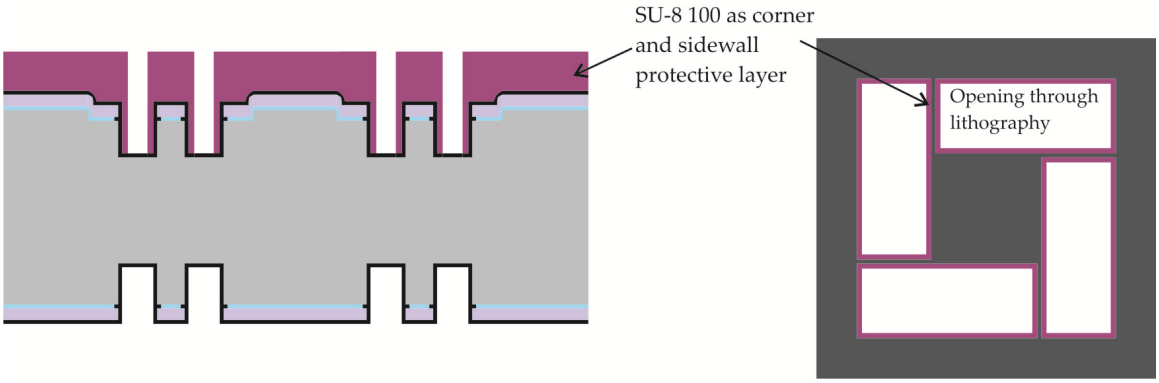
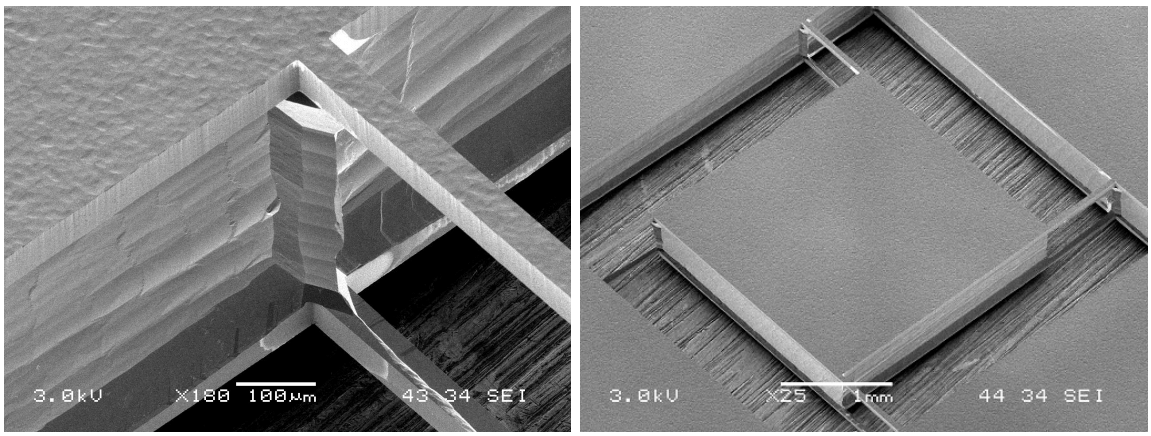


Figure 4.7: SU-8 100 as sidewall protecting layer (a, left) Cross sectional view of partially etched cavity in silicon using SU-8 100 as mask material. (b, right) Top view of new mask with SU-8 100



(a) (b)

Figure 4.8: SEM images showing (a) released springs after wet anisotropic etching of silicon, (b) top view of plate with springs at each corner.

During DRIE of silicon, Reactive Ion Etching (RIE) lag is unavoidable when there is a large difference in the gap widths. For that reason, additional etching time is needed in order to etch through the silicon for smaller gap width structures. The difference in gap

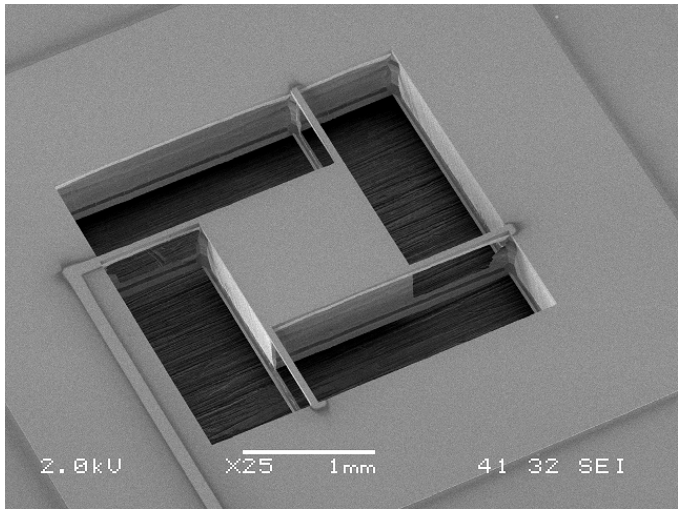


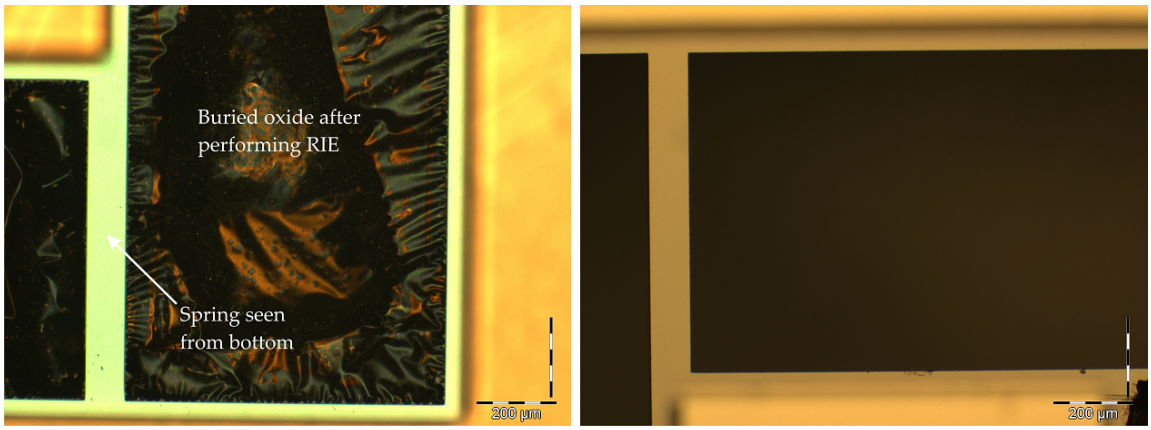
Figure 4.9: Gold-coated plate and springs connected to the frame

widths arises due to the two different spring structures: L-shape and simple beam springs (see Figure 3.4 in Chapter 3). The L-shape spring structures resulted in narrower gap widths as opening with the use of SU-8 100 lithography, whereas the simple beam springs have wider gap widths as the opening as shown in Figure 4.7 (b). For L-shape spring, it was not always successful to etch completely through the silicon with the additional etching time. The over etching time of silicon also destroyed the simple beam spring structures. Therefore it was decided to etch the silicon so that the simple beam spring structures are completely etched through. This is done in order not to lose both the structures, and is resulted in complete etching of silicon to isolate the simple beam spring structure, but not L-shape spring structure. The process then continued with the removal of SU-8 in piranha, followed by the wet anisotropic etching of silicon in 25% TMAH, as explained in Section 4.1. Figure 4.8 shows the SEM images of released structure after removal of all the oxide and nitride layers in 50% HF.

Prior to gold deposition, the silicon is oxidised to get a thin layer of SiO_2, with a thickness of about 10-20 nm in order to prevent formation of eutectic gold-silicon alloy. Later, gold was sputter deposited on the plates and spring areas using a shadow mask wafer [11]. Figure 4.9 shows a SEM photograph of the final chip where the plate and springs are coated with 100 nm of gold.

4.4.2 Results and Discussion of SOI Process

As discussed before, the SOI based process resulted in the successful realization of parallel plates separated at sub-micron distance. However, the steps such as DRIE of silicon handle layer followed by the buried oxide removal and the bonding procedure required optimisation. During silicon handle layer etching (as described in step 7, Figure 4.5), the front side was covered with DuPont Mx5000 foil in addition to the resist. This is used to prevent the springs and plates from being damaged and also to prevent the leakage of Helium into the etching chamber through the wafer holder. However, since the device side or front side consisted of 50 μm deep etched structures; it did not give suitable adhesion of foil to the surface. The removal of foil after etching is more cumbersome as the foil sticks to the surface during etching process. As an alternative, a thick photoresist is used on the front side to protect the device and also to prevent leakage of He, after which the process continued with the etching of handle layer and the buried oxide.



(a) (b)

Figure 4.10: Microscopic image of (a) buried oxide etching after RIE and (b) complete removal of buried oxide after RIE followed by short etching in 50% HF

A second critical step with this process is the removal of buried oxide after etching the bulk handle layer silicon (Step 7, Figure 4.5). The initial idea was to continue etching of buried oxide using RIE soon after the etching of silicon handle layer in step 7. However, it was observed that the etching of buried oxide with RIE process did not result in the complete etching of the oxide; it left some residue of oxide in the form of buckled or cracked layer, as shown in Figure 4.10 (a). To remove these residues left after RIE the remaining oxide was etched in 50% HF for a very short period, which resulted in the

complete removal of buried oxide, thereby releasing the springs, as shown in Figure 4.10 (b). After this, the resist was removed in Piranha solution and eutectic bonding was performed.

4.5 Bonding and Chip Assembly

In both the fabrication processes, once the processed device wafers are ready with deposited gold on top, the parallel plate structures were realized by bonding two similar wafers, by placing them facing the device area one above the other. To achieve this, the mask design was made in such a way that when two such wafers are bonded together, the top plate fits exactly on the bottom plate, thereby making a complete parallel plate structure. Once bonded, the complete chip was broken apart through the breaking grooves. The bonding needs to be done inside the cleanroom to avoid any dust particles in between the bonded area and also on the device area. As described before, two different bonding techniques were developed:

- Si-Si direct bonding for <111>-oriented silicon wafers based process
- Au-Si eutectic bonding for the SOI based process

Both the techniques are briefly explained in the following sections.

4.5.1 Direct Bonding of Si-Si

Direct or fusion bonding generally means joining of any two materials without an intermediate layer or external force. In principle, most materials bond together if their surfaces are flat, smooth and clean. The principle of this method is simple that when two flat, clean and smooth wafer surfaces are brought into contact, it results in a weak bonding based on physical forces. The physical forces can be van der Waals forces, capillary forces or electrostatic forces [12]. Higher bond energy is required for most practical applications, which can be obtained by an appropriate annealing step, which for commercial SOI production is frequently performed at temperatures as high as 1100^{o}C. For this research studies, annealing at higher temperatures is restricted due to the presence of gold on the devices and for electrical connection. Therefore, the direct bonding at room temperature and in a clean environment to avoid dust particles on the surfaces has been used. The resulting adhesion between the two wafers is defined by van der Waals interactions or

hydrogen bridge bonds, which are one or two orders of magnitude weaker than typical covalent bonds. The fabrication process based on <111>-oriented silicon substrates though

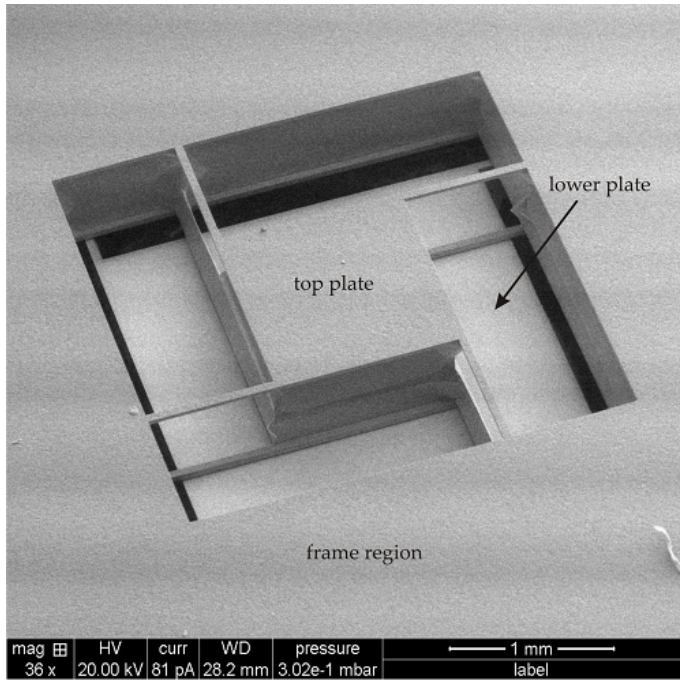


Figure 4.11: SEM image showing the top view of bonded top and bottom plates

resulted in realising the top and bottom plates, however, it was not possible to achieve the wafer scale bonding. Since the breaking grooves were not etched completely during through wafer etching of silicon, bonding two wafers and then break the bonded stack would be much more difficult. Therefore, at first the top and bottom plates are separated apart and then bonded those together on chip level to make the complete parallel plate structure. Figure 4.11 shows SEM image of bonded top and bottom plate structure. Since heating at higher temperature is not suitable, an adhesive was used at the sides of two bonded plates to keep them intact. Further steps of assembling the bonded parallel plate chip in PCB is explained in following sections.

4.5.2 Eutectic Bonding of Au-Si

Once the processed wafers are ready with released spring structures, two similar wafers are aligned and placed with their device structures facing each other. At the contact interface of the two wafers, gold on top of polysilicon layer is present, as shown in the cross section of two bonded plates in Figure 4.1 (d).

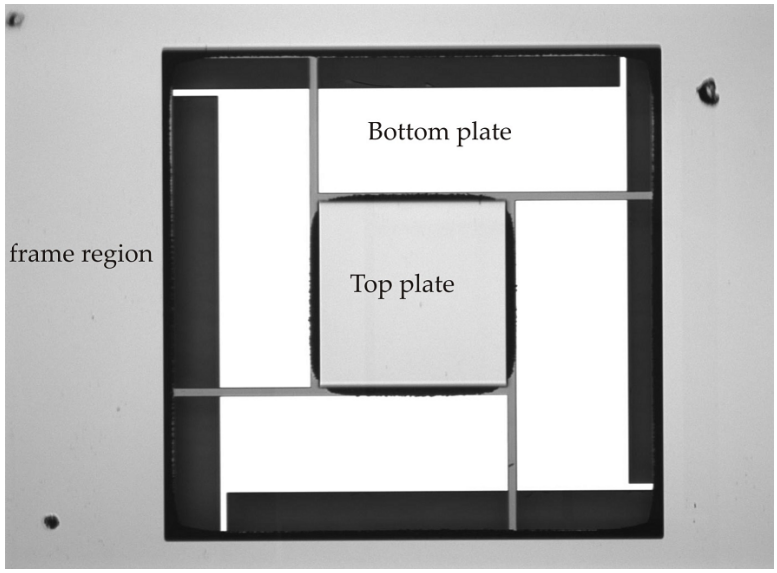
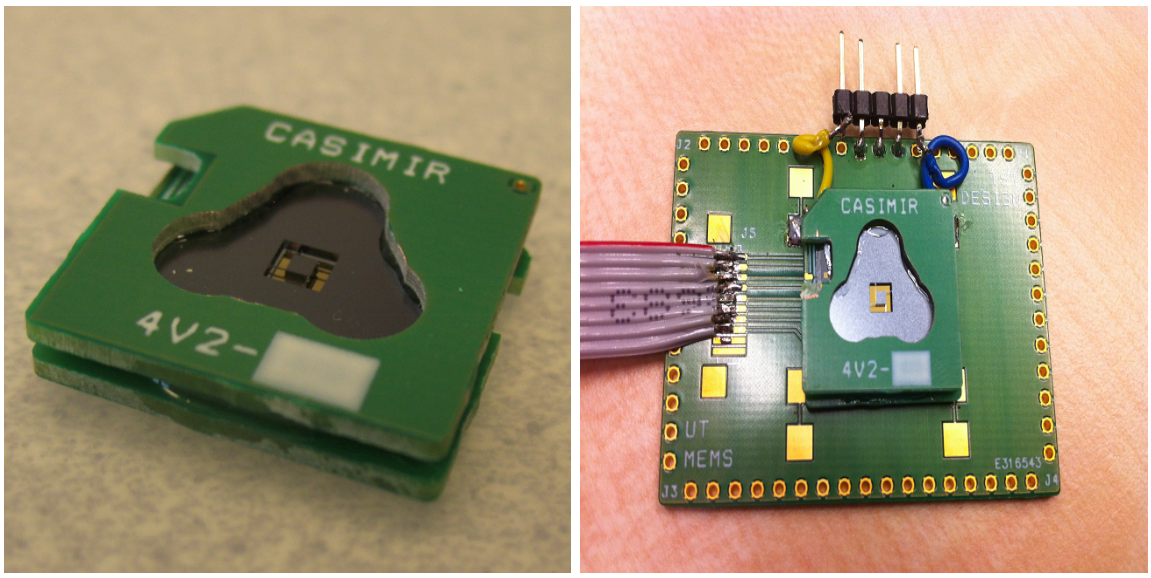


Figure 4.12: Microscopic image showing the top view of bonded top and bottom plates

When they are heated at a temperature higher than the eutectic melting point, the contacted surface layer containing the eutectic composites melts, forming a liquid phase alloy. This accelerates mixing processes and diffusion until the saturation composition is reached. Ultimately, this phenomenon results in the formation of a thicker Au-Si alloy layer leading to a stronger eutectic bond [13, 14]. The chips are then broken apart at the break-lines, which were also etched in steps 4 & 8 in SOI process as shown in Figure 4.5 (a). Figure 4.12 shows the microscopic image of a realized bonded structure as seen from top.

4.5.3 Assembly of Chips

The procedure to assemble parallel plate structures for the measurement is same for the devices realised using both the <111>-oriented substrate and SOI processes. The silicon chips are carefully assembled in a module using thin printed circuit boards (PCB) at either side for connection of the gold electrodes by wire bonding and protection of the fragile spring structures.



(a) (b)

Figure 4.13: (a) Photograph showing the silicon chip mounted between two thin PCB's & (b) a complete assembled sensor module.

The silicon chips connected to thin PCB is shown in Figure 4.13 (a). The entire module is mounted on a third PCB containing the piezoelectric actuators. The piezoelectric actuators are glued to the main PCB and characterized before mounting the sensor module. The piezoelectric actuators allow a displacement in the order of 2 μm at the maximum voltage of 100V, which in this case is sufficient to close the gap between the parallel plate structures. Figure 4.13 (b) shows the complete assembled parallel plate chip on PCB containing piezoelectric actuators.

4.6 Conclusion

Fabrication processes based on two different substrates were developed to realize the parallel plate structures for Casimir force measurement. The fabrication process based on <111>-oriented silicon substrate is devised to make plates with smooth surfaces. This is based on a combination of DRIE and wet anisotropic etching of <111>-oriented silicon substrates, which resulted in ultra smooth surfaces ending at <111> plane when etched in wet anisotropic etchant like TMAH. The second fabrication process is mainly developed to have good yield and a reproducible way of realizing parallel plate structures with sub-micron separation distance between them. Both the fabrication processes resulted in realization of parallel plate structures, the devices based on SOI process were successful to perform measurements.

A qualitative comparison of both the processes is given in Table 4.1. The high temperature processes are of significant relevance, which tend to induce thermal stress in the structures that needs to be taken care of. The critical steps include challenges like the uniformity of a layer, etch profile, selectivity and alignment. Additional accessories are the ones which are used with the device wafers such as carrier wafer and shadow mask wafer. In <111>-oriented process, for DRIE of silicon (as given in step 12, Figure 4.3) a carrier wafer is necessary to hold the device wafer in order to etch through the silicon wafer. A shadow mask technique is used to deposit gold on plates and springs connecting to the electrical bondpad, for which an additional wafer has been processed. These steps are not included in the process steps of the fabrication scheme directly; however, they were processed in parallel with the device wafers.

The reliability of <111>-oriented substrate process is mainly challenged with the DRIE of silicon in step 12, Figure 4.3. The process is reliable, when SU-8 100 is used as an alternate sidewall protecting layer. Although the processing of SU-8 100 also required further optimization, it proved to be robust to withstand the longer etching run, which was highly essential in <111>-oriented substrate based fabrication. The device wafers underwent processing with SU-8 100 several times during optimization process; this does not leave any additional surface roughness and also no bending due to stress evolved during the SU-8 processing. This makes it a worthy alternative approach to protect the devices during the etching of silicon through wafer.

The second fabrication process based on SOI substrate discussed in this Chapter resulted in the successful realization of parallel plate structures with defined separation distance. Despite the fact that the surface roughness of the plates was not quite as smooth

Table 4.1: Qualitative comparison between <111>-oriented substrate process and SOI process

Parameter	<111> process	SOI process
Number of masks	5	3
High temperature process (>500^{o}C)	9	2
Critical steps involved	6	3
Additional accessories	2	0
Reliability of process	Poor	Good
Reproducibility of process	Not sure	Possible
Overall difficulty of process	High	Average
Yield	<100%	$\sim$ 100%
Strength of Bond	Average	Strong
Surface roughness	Good	Average

as in <111>-oriented silicon process, the yield and reproducibility of the process has been promising. The plates have one sided spring, which reduces the complexity of fabrication; however this has to be remunerated with the reduced mechanical stability. The Au-Si eutectic bonding resulted in a strong bond between the plates that the initial distance between the plates remained in the order of $\sim$1 μm. In comparison for the <111>-oriented substrate process, the direct Si-Si bonding, though doesn't require further processing like heating in oven, it is highly desirable to have highly polished and ultra clean surfaces to have strong bond.

For an overall perception, the process based on <111>-oriented substrates with the additional process steps could still result in plates with smooth surface which is one of the prime requirements in the Casimir force measurement. However, this process is challenged with many critical steps, besides, the lengthy process also makes it a less viable choice. Whereas the SOI process appears more promising in terms of easiness of the process and the strong metal-silicon eutectic bonding of plates that results in sub-micron separation distance, which could make it a more practical choice to realize the parallel plate structures.

4.7 References

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Chapter 5

Casimir Force Measurement: Experimental Verification

Synopsis

This chapter presents the results of experimental work towards the measurement of the Casimir force. The devices realised using the two fabrication schemes as described in Chapter 4 are used for the initial characterization and measurement. The initial characterization of the devices is performed at both atmospheric pressure and vacuum ambiences. The measurement results at vacuum environment show the expected opposite phase movement of the top plate, however the measured amplitude is too large to be caused by the Casimir force. Further analysis and more measurements will be needed to uncover the exact cause of this large vibration amplitude.

5.1 Introduction

In this Chapter, the experimental testing of the measurement principle described in Chapter 3 with the realised MEMS parallel plate structure is studied. Prior to bonding, the devices were studied for the surface roughness and waviness. The surface roughness will ultimately limit the lowest possible separation distance at which measurements can be performed. With the devices based on <111>-oriented substrate process, although the chip breaking and bonding appeared successful, during initial measurements it was found that the separation distance had increased to more than 2 μm. Increase in the separation distance might be due to the presence of particles or the diffusion of glue (used at the sides of the plates to assist the bonding) in between the chips which did not result in the strong bonding of the top and bottom plates and ultimately increasing the separation between them. As a result, the gap between the plates was far too large for the piezoelectric actuators, rendering the devices unsuitable for the Casimir force measurement. However, this process resulted in plates with smooth surfaces with a measured surface roughness in the order of 3 nm RMS as presented in this chapter. Furthermore, the preliminary experimental results with the devices based on SOI substrates are presented in this Chapter. The piezoelectric actuators are also characterised in order to choose the piezoelectric actuators having almost identical behaviour and displacement.

This Chapter is organised as follows. In the next section, a brief introduction on the measurement system, a Polytec Vibrometer, used for different measurements involved in this Chapter is given. Before bonding the plates, the surface of both plates is analysed to estimate the surface roughness and waviness and their result is discussed in Section 5.3. In Section 5.4, the characterisation of piezoelectric actuators used in the experiments is presented. After these initial characterizations, the parallel plate structure is studied to estimate the resonance frequency of top plate. The result of this experiment is discussed in Section 5.5. In the same section, the experimental results obtained when attempting to measure the Casimir force are explained in detail. A discussion on the obtained experimental results is presented in Section 5.6 and finally general conclusions are given in Section 5.7.

5.2 Measurements using Vibrometer

The experiments discussed in this Chapter are performed using a Polytec MSA-400 Micro System Analyser [1]. The MSA-400 Micro System analyser is a measurement tool for

the analysis and visualisation of structural vibrations and surface topography in micro structures such as MEMS. It consists of a fully integrated microscope with a scanning Laser Doppler Vibrometer (LDV), Stroboscopic Video Microscopy (SVM) and scanning White Light Interferometry (WLI) [2]. The measurements discussed in this Chapter are performed using LDV and WLI. Operation of the LDV is based on the Doppler effect; sensing the frequency shift of back scattered light from a moving surface.

In general, an LDV is best suitable for measuring non-contact vibrations by directly measuring the velocity as well as displacement. Using suitable interpolation technique, the Polytec vibrometer can reach a resolution of 2 nm and with a digital demodulation technique; it can reach down to picometer range. Using LDV, the characterisation of piezoelectric actuators and the experimental verification of Casimir force are performed. With WLI, the surface topography data such as determination of structure height and shape on both rough and specular surfaces can be analysed. The WLI works on the principle of Michelson interferometer. Using WLI, the surface profile to estimate the surface roughness and waviness of the fabricated top and bottom plates are studied before they are bonded together.

5.3 Surface Roughness

In this section, the surface roughness and waviness of both the top and bottom plates are studied. The roughness and quality of the deposited gold layer can influence the measured Casimir force significantly. From the earlier experiments, it was observed that surface roughness increases the actual Casimir force, leading to systematic errors in the measurements [3-5]. The surface roughness also introduces a lower limit on the separation distance in the parallel plate geometry [6].

Even upon contact, the surfaces are still separated by a distance defined by the roughness of the plates. Therefore, before bonding the plates, the surface roughness was measured using both AFM and white light interferometry, as given in Figure 5.3. At submicron scale the surface roughness is completely defined by the sputtered gold layer as shown by the AFM measurements in Figure 5.1. Without the gold layer it is below 1 nm, both before and after oxidation. After deposition of the 100 nm thick gold layer it increases to about 3 nm RMS.

At larger scale, for instance on the plate surface area (1000*1000 μm^2), it is seen that the waviness of the silicon surface dominates the roughness which is in the order of

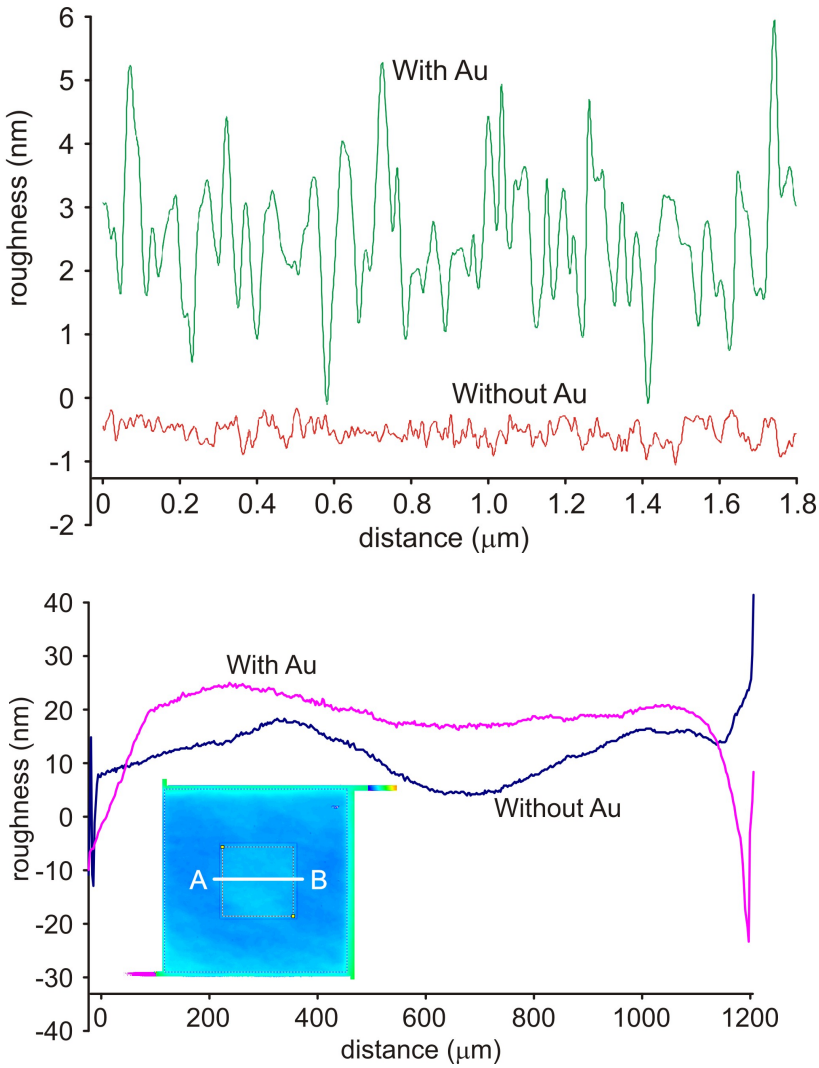


Figure 5.1: (a, top) roughness measurement over a distance of 2 μm using AFM & (b, bottom) waviness over a distance of 1200 μm using White Light Interferometer

10-20 nm over a distance of 1200 μm. This waviness may result in the non-parallelism of the surfaces under interaction, which may result in the increased Casimir force [7]. Figure 5.2 shows the deviation of one of the plates due to inhomogeneties in the plate surface. The Casimir force increases if the split between the surfaces is a convex-convex or concave-concave lens. In those cases, the force can be measured as [7]:

$$F = F_{CL}\left[1 + \frac{10}{3}\left(\frac{H}{d}\right)^2 + 7\left(\frac{H}{d}\right)^4\right] \tag{5.1}$$

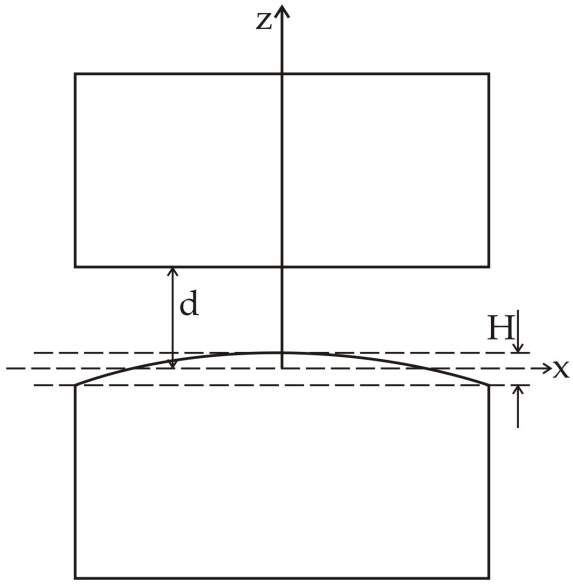
Where F_{CL} is the measured Casimir-Lifshitz (CL) force as described in Equation 3.6, H is the amplitude of deviation and d is the average separation distance between the plates. In the current case, the surface roughness is in the order of 20 nm and using this as a value for H, the increase in force due to non-parallel geometry is shown as % error in Figure 5.2(b). The error is plotted against varying distance between the plates. From the graph, it can be seen that the % error increases with decreasing distance between the plates.

5.4 Characterisation of Piezoelectric Actuators

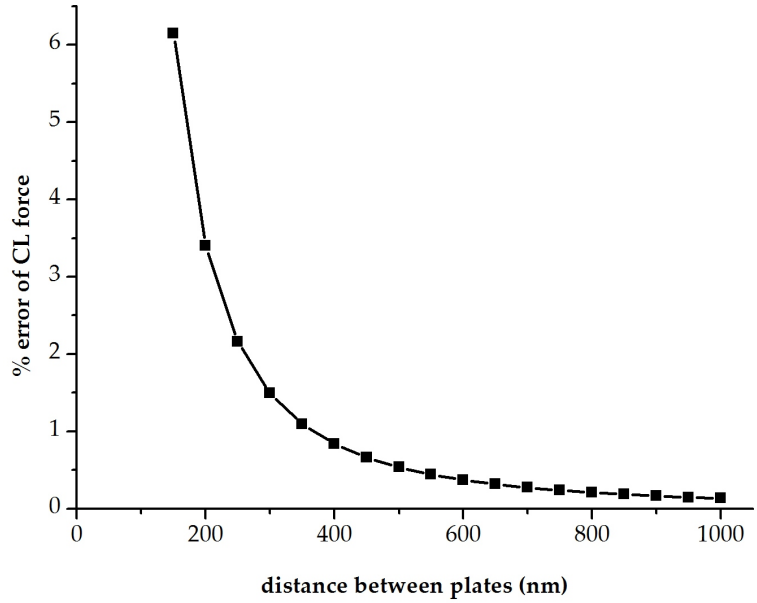
The piezoelectric actuators used in the experiments are Ceramic Insulated high-power actuators from PI (Physik Instrumente GmbH & Co) [8]. These actuators are sized as 2x2x2 mm, which are the smallest monolithic multilayer piezo stack providing sub-nanometer resolution and sub-millisecond response. The piezoelectric actuators are characterised using Polytec Laser Vibrometer and the White light interferometry.

The top surface of the piezo actuator where the lower plate of the parallel plate structure is placed is scanned completely to study the behaviour of vibration and also to measure the displacement per volt. To do so, the piezoelectric actuator is actuated with a sinusoidal signal of 2 kHz with 1 V_{pp} (peak to peak voltage) and the entire top surface of the piezo actuator is scanned under Laser vibrometer. With an increasing voltage, the increase in the displacement of the piezoelectric actuator is measured. Displacement of piezoelectric actuator as measured by vibrometer is shown in Figure 5.3 for two different actuation voltages, V_{ac}.

Figure 5.4(a) shows the increase in the displacement of piezo with increasing AC voltage and Figure 5.4 (b) shows the displacement for constant V_{ac} and varying V_{dc}. The measured displacement was in the order of $\sim$10 nm per volt. To assemble a chip

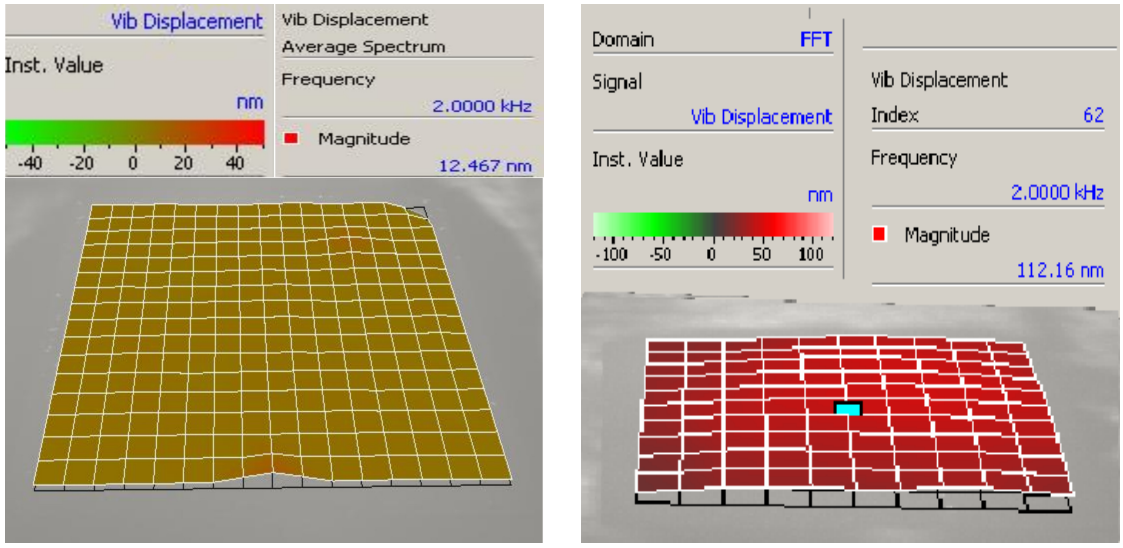


(a)



(b)

Figure 5.2: (a, top) Parallel plate configuration with paraboloidal deviation at one plate [7] & (b, bottom) % error of CL force as calculated using Equation 5.1



(a) (b)

Figure 5.3: Vibrometer result showing the average displacement of piezo actuator for different actuation voltages, for (a) V_{ac}= 1V and for (b) V_{ac}= 9V

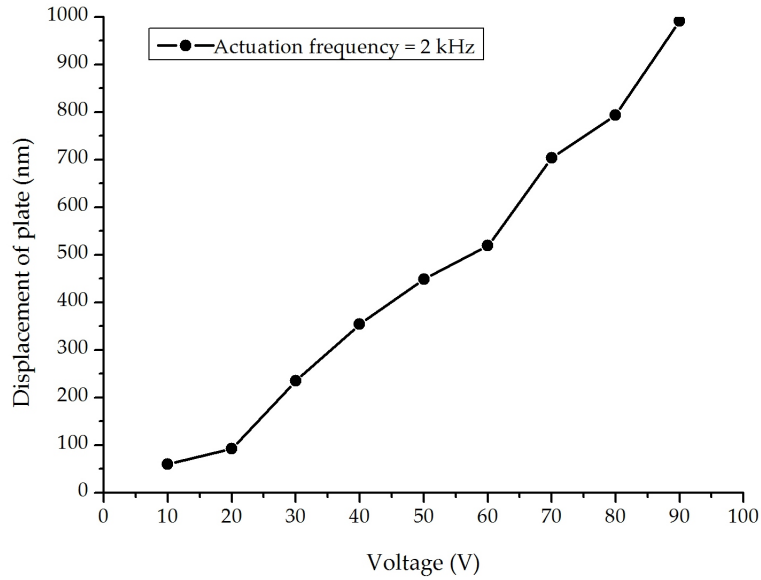
comprised of parallel plate structures with piezo actuators to perform the Casimir force measurement, 4 piezo actuators are required: one to actuate the lower plate and the other 3 at the frame region of the chip to maintain the parallelism between the plates. The piezoelectric actuators assembled on a PCB are shown in Figure 5.5. All these piezo actuators are individually studied and are selected based on having displacement in the order of 10 nm per volt.

5.5 Preliminary Experimental Verification

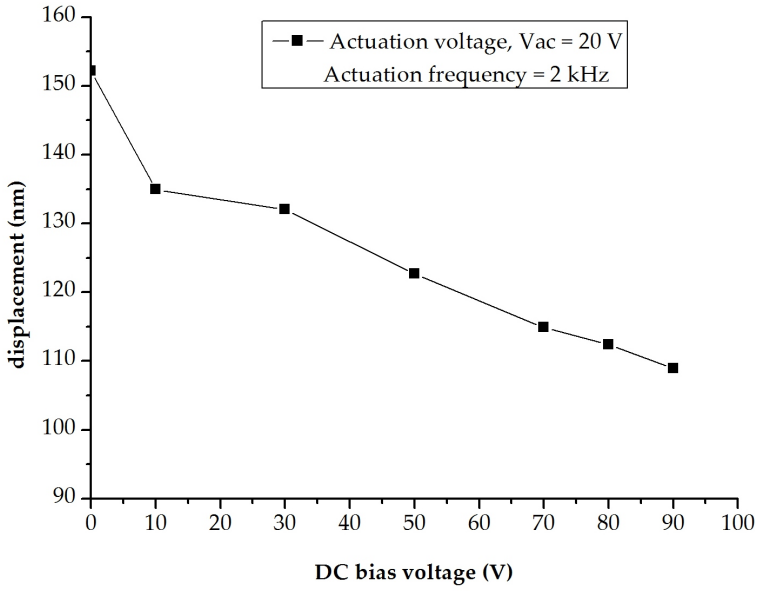
The bonding of top and bottom plates followed by the chip assembly and wire bonding are performed as described in Section 4.5.3, Chapter 4. After chip assembly and wire bonding are performed for connections, the devices are initially checked for any electrical contact between the top and bottom plates by measuring the contact resistance between them.

5.5.1 Resonance Frequency Measurement

The resonance frequency measurement gives the estimation of the spring stiffness of the mass-spring structure of the top plate. For the CL force measurements, the lower plate



(a)



(b)

Figure 5.4: (a, top) Measured displacement of piezoelectric actuator for varying applied voltage, V_{ac} and (b, bottom) measured displacement of piezoelectric actuator for constant V_{ac} and varying V_{dc}

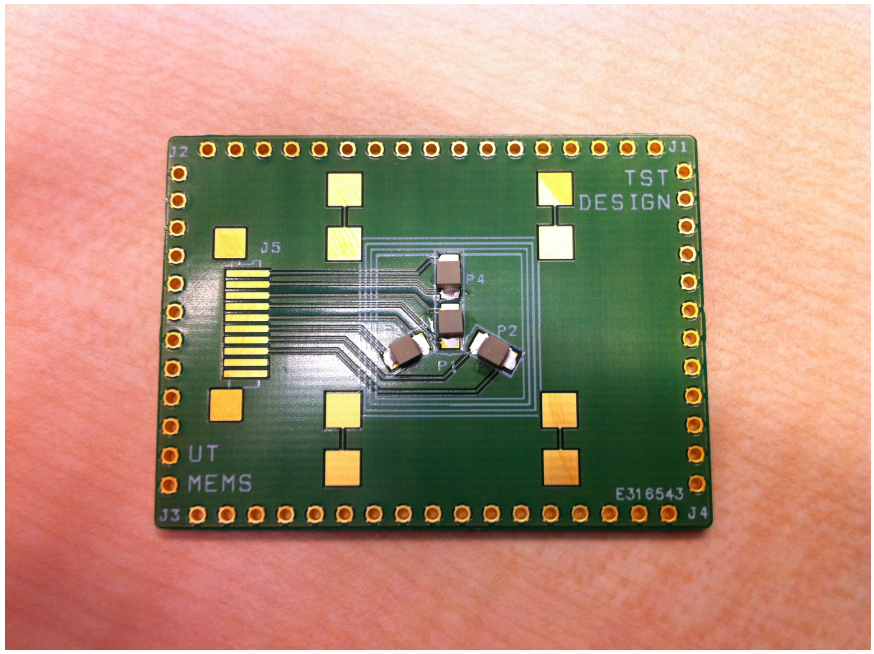


Figure 5.5: Piezoelectric actuators assembled on PCB for characterisation

is actuated with a frequency lower than the resonance frequency of top plate. Therefore it is essential to estimate the resonance frequency of the plate. To avoid effects due to damping, the resonance frequency measurement was carried out in vacuum chamber at a pressure of $7.4\text{x}10^{-6}$ mbar. Initially, the piezoelectric actuator is actuated by 5 V periodic chirp signal. Further, a small DC voltage is applied between the plates and both the top and bottom plates along with the rim or frame region (where both the plates are bonded) were scanned.

Figure 5.6 shows the scanned result as obtained from vibrometer. Here the frequency is chosen to be the resonance frequency of top plate; hence the top plate amplitude is at maximum. The measured top plate resonance frequency is 14.242kHz, which matches well with the designed value of 14.478 kHz. The result of frequency response of the top plate is shown in Figure 5.7. From this result, it is observed that there is no other resonant mode in the frequency range below 15 kHz. Further, from the scanned results, it was observed that the frame region/rim (where both the plates are bonded) is not moving, which confirms that there is no mechanical coupling between the plates through the frame region.

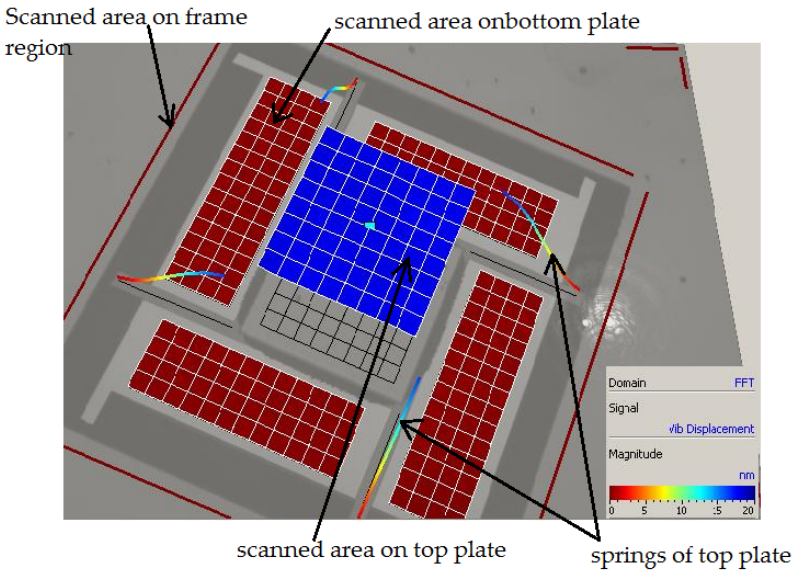


Figure 5.6: Scanned result showing the difference in the vibration amplitude of top plate, bottom plate and the frame region

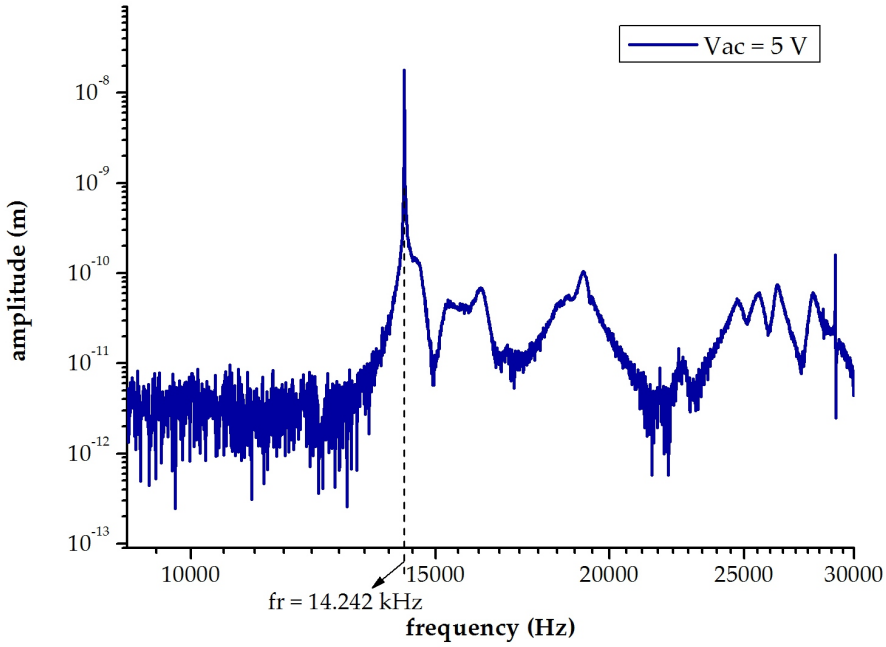


Figure 5.7: Frequency response of top plate showing the resonance peak as measured by Laser Vibrometer (log-log scale)

5.5.2 Towards Casimir Force Measurements

The measurement principle presented in Section 3.2, Chapter 3 was used for the CL force measurement, where the entire top plate, part of the bottom plate and the rim region are scanned by laser light for the measurement. As explained in Chapter 3, the CL force is measured in terms of displacement of top plate; for which, various methods to measure the displacement as described in Chapter 3 are implemented for experimental verification. The measurement principle was verified by performing the measurement at atmospheric pressure and at lower pressure down to 7.4x10^{-6} mbar. All measurements were done at room temperature (approximately 20 degrees Celsius)

Measurement at Atmospheric Pressure

The CL force measurement at atmospheric pressure is carried out to evaluate the coupled movement of both the plates due to the thin layer of air between the plates. Upon actuation of the lower plate, the resulting movement of the top plate followed the same phase as that of lower plate. Thus, confirming that the top plate movement is solely due to the air-coupled movement. To verify this, the piezoelectric actuator beneath the lower plate is actuated with a frequency far below the resonance frequency of top plate. In this case, a 5 kHz sine signal with 1 V_{pp} is used for actuation and both the top and bottom plate area are scanned. From this measurement, the following results are observed:

- The resulted actuation amplitude of lower plate was in the order of 4nm and the top plate amplitude in the order of ∼18 pm.
- Both the plates movement are in-phase with respect to each other.
- Actuation with different frequencies say 3 kHz, 5 kHz or 7 kHz (still keeping it far below resonance frequency of top plate) does not change the vibration amplitude of both the plates, whereas actuation with increased V_{pp} resulted in higher amplitudes of vibration for both the plates.
- The in-phase movement of both the plates is due to the air dominated coupling between the plates.

The measurement result from the vibrometer is shown in Figure 5.8, where the colour difference in the magnitude shows the difference in the amplitudes of top and bottom plates and the similar colour in the phase measurement shows both the plates having same phase of movement.

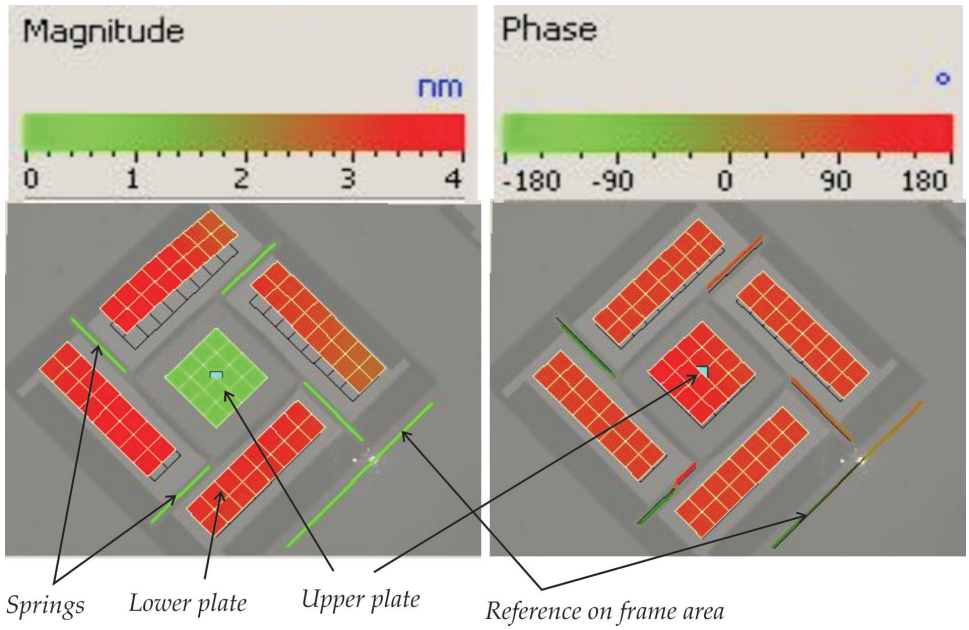


Figure 5.8: (a) Top view showing the scanned results of vibration amplitudes of both the plates using laser vibrometer, (b) Image showing in- phase movement of both the plates as measured in Laser vibrometer. In (a) difference in colour shows the different vibration amplitude of both the plates: the measured lower plate amplitude was 4 nm for 1 V_{pp} which resulted in the upper plate vibration amplitude in the order of 0.018 nm, wherein (b) is the in-phase movement of both plates

Measurement at Lower Pressure

At lower pressure of 7.4x10^{-6} mbar, the lower plate was actuated again with a 1 V_{pp} actuation voltage at 1 kHz. In this case, the upper plate vibrated in opposite phase with respect to the lower plate, as shown in Figure 5.9. However the measured vibration amplitude of the upper plate is extremely small, due to the low vibration amplitude of the actuated plate and the large initial separation distance of $\sim$1 μm. The measured vibration amplitude of lower or actuated plate was in the order of 4 nm which resulted in the quite low vibration amplitude of upper or response plate as 0.01 nm. In order to increase the vibration amplitude of top plate, the lower plate was actuated with higher V_{pp} voltage such as V_{pp} = 20 V. With such actuation voltage, the resulted vibration amplitude of lower plate was 70 nm and the top plate displacement was 0.29 nm. Figure 5.9 shows the measured results of both the lower and upper plates. In Figure 5.9, the colour difference in (a) shows the magnitude of vibration of top and bottom plates and the colour difference in (b) shows the difference in the phase of top and bottom plates. From this initial measurement at lower pressure in vacuum chamber, it was inferred that the device behaves as expected.

To tune the separation distance between the plates, a DC bias voltage is applied to the piezoelectric actuator in addition to the AC actuation voltage, in order to decrease the distance between the plates. As a result, the force between the plates should increase, which in turn can increase the vibration amplitude of the upper plate. After initial measurement in the vacuum chamber at lower pressure, further measurements are performed by applying a DC bias voltage to tune the separation distance. By considering initial separation distance, d_0 of 1 μm and displacement of 10nm/volt, the change in distance between the plates, d_i is given as:

$$d_i = d_0 - \alpha V_{dc} \tag{5.2}$$

where α is the sensitivity of piezoelectric actuator which is about 10 nm/V and V_{dc} is the varying DC bias voltage to the piezoelectric actuator.

The Casimir force formula described in Equation 2.1 is dependent on the distance (d) and surface area of plate (A), which gives the static force between the plates. The varying force which results in the change in position due to an AC signal can be calculated from

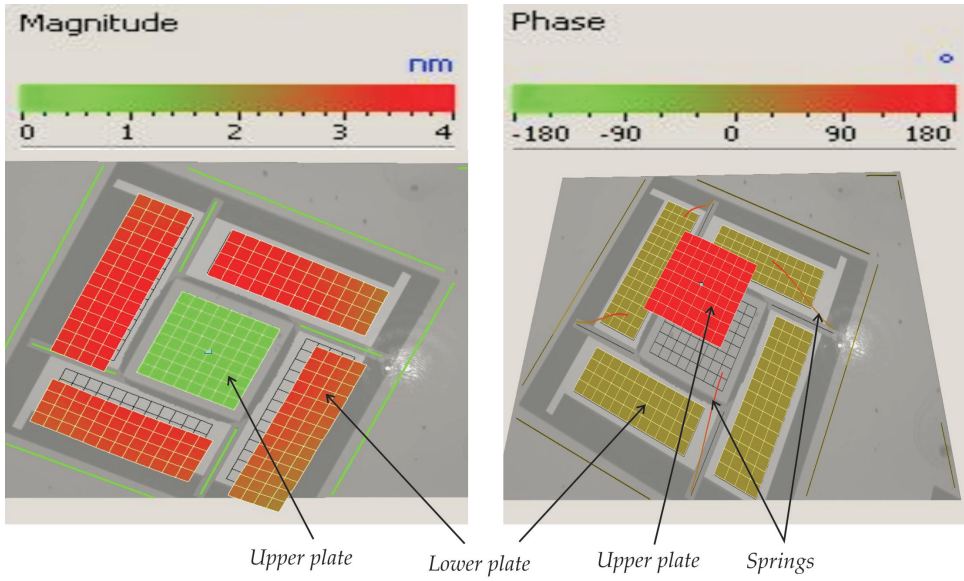


Figure 5.9: (a) Top view showing the scanned results of vibration amplitudes of both the plates using laser vibrometer, (b) Image showing out of phase movement of both the plates as measured in Laser vibrometer. In (a) difference in colour shows the different vibration amplitude of both the plates: the measured lower plate amplitude was 4 nm for 1 V_{pp} which resulted in the upper plate vibration amplitude in the order of 0.01 nm, however (b) is the opposite phase movement of both the plates

the following equation:

$$\Delta F_{CL} = F_{CL}(d_i - amp, A) - F_{CL}(d_i, A) \tag{5.3}$$

where ΔF_{CL} is the increase in Casimir-Lifshitz (CL) force when the plate separation changes from d_i to $d_i - amp$ and which is a dependent on the amplitude of vibration, amp, varying distance between the plates, d_i and the surface area of the plate, A. $F_{CL}(d_i, A)$ is given by:

$$F_{CL}(d_i, A) = 13 \cdot 10^{-6} \left(\frac{A}{1mm^2}\right) \left(\frac{d}{100mm}\right)^{-4} \tag{5.4}$$

As mentioned in Chapter 3, the CL force is measured in terms of displacement of top plate, which can be obtained as:

$$x_i(amp, d_i, A) = \frac{FC(amp, d_i, A)}{K_{eff}} \tag{5.5}$$

where K_{eff} is the effective or total stiffness constant of the 4 springs connected to the top plate as given in Equation 3.5.

For the initial measurement described above, the calculated displacement values for the actuation amplitude of 70 nm for different separation distances such as 200 nm, 600 nm and 1000 nm are presented in Figure 5.10. In the Figure 5.10, the calculated displacement of top plate is in the order of tens of picometers for larger separation distance viz. 1000 nm and is in the measurable range of vibrometer. In the experiment, the measured top plate displacement is normalised with respect to the displacement of lower plate which can be given as:

$$x_{norm} = \frac{x_t}{x_b} = \frac{x_t}{Z_{act}} \tag{5.6}$$

where x_{norm} is the normalised displacement, x_t is the displacement of top plate, x_b is the displacement of bottom plate, which is equivalent to Z_{act}, the actuation amplitude in Equation 3.10.

Further measurements were performed by applying a DC bias voltage which is gradually increased from 0 to 70 V. 70 V is chosen in order to be within the threshold limit of the piezoelectric actuator, which could withstand the maximum voltage of 100 V. With an increasing DC bias voltage up to 60 V, the phase measured between the lower and top plate was always $\sim 180^o$, which shows that they both move towards each other in opposite phase. However, at DC bias voltage = 70 V, both the plates moved in-phase, which could be that the plates start touching each other. Moreover, the measured top

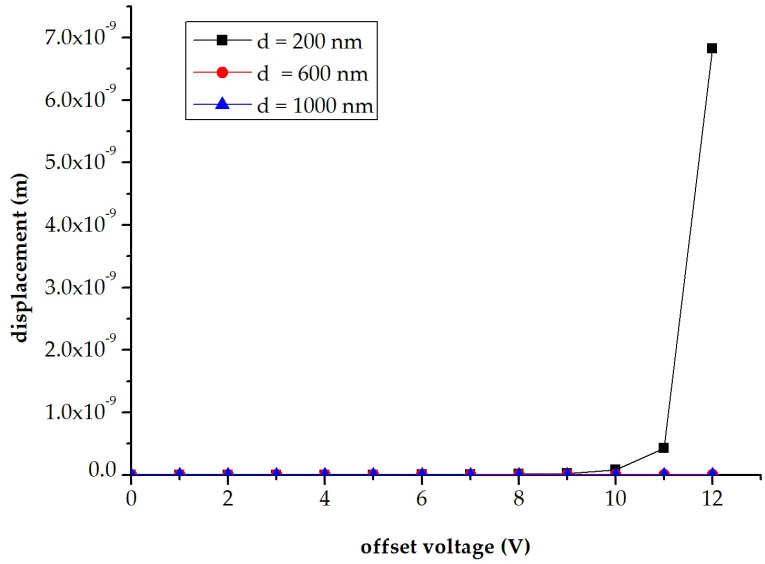


Figure 5.10: Calculated top plate displacement as a function of varying of offset voltage for three different separation distances

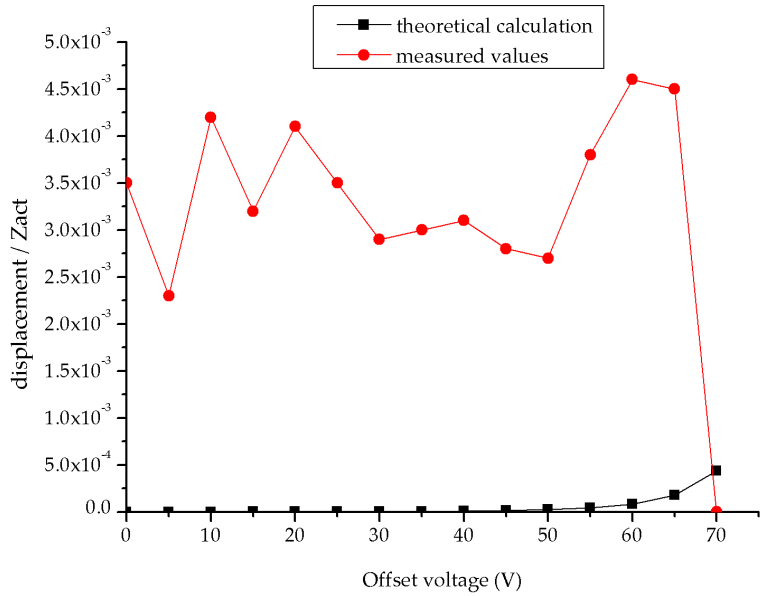


Figure 5.11: Measured and calculated normalised top plate displacement as a function of increasing DC bias voltage

plate displacement did not follow the d^4 dependency.

The measured top plate displacements which are normalised with the lower plate amplitude are presented in Figure 5.11, where the normalised displacements are plotted against the varying DC bias voltage. Also shown in Figure 5.11 is the calculated normalised top plate displacement. From the Figure 5.11, it is observed that the measured values are higher than the theoretical values and does not follow a trend with an increasing DC bias voltage. Further, as observed from the frequency response of top plate shown in Figure 5.7, there is no other resonance peak in the frequency range below 15 kHz. This confirms that the large amplitude of vibration (shown in Figure 5.11) measured is not due to resonance.

5.6 Discussion

Initial characterisation of the fabricated MEMS chip to measure the Casimir force is presented in this Chapter. The device based on <111>-oriented substrate process resulted in ultra smooth surfaces measuring a roughness in the order of ∼3 nm RMS and the waviness in the order of ∼20 nm. However, these devices could not be used with the measurement of the Casimir force due to the increase in the separation distance between the plates.

Devices based on SOI process resulted in strongly bonded parallel plates separated at $\sim 1\mu$m distance. With this device, the initial measurements were performed to verify the principle of Casimir force measurement. The initial measurement results show that the device behaves as expected. Based on this result, further measurements were carried out to verify the dependency of top plate displacement on distance to the power four, d^4. The experiments result showed out of phase movement of both the plates with respect to each other, however, the measured top plate displacement did not follow d^4 dependency. Besides, the measured top plate displacements are larger than the predicted theoretical values.

From the experiments discussed in this chapter, the followings are to be noted:

- The piezoelectric actuator is driven with frequency far below any resonance in the system, which confirms that the large amplitude of vibration measured in the experiments shown in Section 5.4.2 is not due to resonance.
- In all the experiments performed, the rim of the top plate did not move with measurable amplitude.

- Up to certain applied DC bias, the top plate itself moved in opposite phase with respect to the bottom plate. This movement can not be induced through the suspension, because the driving frequency used for actuation of lower plate is far from any resonance of the whole system. Therefore the only possibility of such movement is due to an attractive force between the plates.

- The increase in the displacement of the top plate due to the force between the plates does not follow d^4.

- From the measured amplitude of vibration of top and bottom plates, the distance between the plates could be estimated and it is found to be ∼160 nm. This implies that the distance between the plates has reduced to a very small value. It could have happened due to the use of glue to fix the lower plate on the piezoelectric actuator, which pushed the bottom plate upwards, thereby reducing the distance between the plates.

- The calculated top plate displacement with $Z_{act} = 70$ nm for a separation distance, d of $\sim$ 160 nm does not match with the measured values of amplitude of top plate, which are relatively large.

- Further, it was inferred that the amplitude of top plate is independent of the applied DC bias.

The measurement results discussed in Section 5.5.2 does not follow any trend and it needs to be studied further to understand clearly. Further, the large amplitude of top plate vibration and the non-dependency of it on the DC bias are also unclear to be compared with theory. This demands for more measurements to demonstrate the measurement principle using the developed parallel plate chip.

5.7 Conclusion

The successfully fabricated MEMS chip has been employed to demonstrate the principle of Casimir force measurement using parallel plate geometry. The measurement principle using micromachined chip could open up future possibilities for the experimental investigation of Casimir force between parallel plate geometry in a more improved methodology. However, to materialise the measurement of the Casimir force with the MEMS chip described in this thesis Chapters 3, 4 and 5, more measurements with the new devices are

necessary. In the MEMS parallel plate chip assembly set-up used in this thesis study, glue was used to fix the parallel plates on the piezoelectric actuator. For future experiments, it is probably better to use a clamping system to mount the parallel plates on the piezoelectric actuator.

5.8 References

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Chapter 6

Towards a Fast Mechano-Optical Modulator: Principle and Design Methodology

Synopsis

A mechano-optical modulator based on the Integrated Optical Nano-Mechanical (IONM) effect is devised. Though based on this effect, a multitude of devices have already developed, our design approach is one of its kind that describe the possibility of hybrid integration of a light-weight mechanical element with an optical waveguide, without the need of modifying its properties. Further, a bi-directional electrostatic actuation is envisioned for fast movement of the mechanical element towards the optical waveguide to perform as ON/OFF intensity modulator. In this chapter, the design approach of the waveguide and the mechanical structures are explained in detail that ultimately forms the optical modulator.

6.1 Motivation

Within the MEMS parallel plate structures investigation, one of the main motives is to realize the parallel plates separated at smaller distances which can be used to design structures such as power sensors [1], optical modulators using a mechanical structure in evanescent field [2-4], electro-mechanical tuning and electrical and optical switches [5-6]. Further, within the MEMPHIS project the most important application is optical switching in ring based multiplexers and de-multiplexers [7,8], for which we have focused mainly on the use of parallel plate structures for optical modulation with high switching speed as the main requirement. The optical modulation is based on the IONM effect [9] involving electrostatic force for the bi-directional actuation of the parallel plate structure formed by a hybrid integrated mechanical structure with the optical waveguide.

In general, smaller distances between MEMS components are desirable in electrostatic actuation schemes because they permit smaller voltages to be used to generate larger forces and torques. MEMS currently employed in sensor and actuator technology have component separations on the order of microns and sub-micron distances. The mechanical structure used in this study of Mechano-optical modulator is also need to be operated at sub-micron distance to enable the modulation. At such separation distance the Casimir force will take precedence over its functioning. The experimental study of Casimir force involves the design and conditions favouring its presence, however, in the operation of MEMS and NEMS devices, it has to be avoided. Further, the pull-in instability condition of the parallel plate actuators also needs to be addressed in the design involving parallel plate geometry.

With these requirements, the design study of the parallel plate optical modulator is investigated to realize a fast responding mechano-optical modulator based on IONM effect. In the design study, first the concept of introducing loss in the optical path by moving a metal coated suspended plate is verified using simulations. Later, both the optical waveguide and the mechanical element are studied individually and their design analyses are presented in detail.

6.2 Design of Parallel Plate Mechano-Optical Modulator

The parallel plate mechano-optical modulator comprises of waveguide as one plate and the mechanical element as another plate in parallel to the waveguide. Here, the main aim is to have a fast moving mechanical element which can be integrated with any waveguide to modulate the signal propagating through it. The mechanical structure is integrated with the optical waveguide through hybrid integration, which allows for individual optimization of fabrication processes for both the mechanical structure and optical waveguide. Further, only fewer changes are needed as post processing steps in the fabrication of waveguides. Figure 6.1 shows the top views of the mechanical chip and optical waveguide chip. The suspended plate/beam structure is self-aligned to the waveguide using etched trenches that exactly coincide with the cavity (shown as 3x3 mm^2 in Figure 6.1 (b)) in the top cladding of the waveguide and is connected/clamped to the optical waveguide through the three bondpad/electrodes shown in Figure 6.1. Once connected, the chips are separated by a well-controlled air gap of 1 μm. This air gap is created by a local oxidation process on the mechanical chip. A cross section of an integrated mechanical chip with an optical chip is shown in Figure 6.2. A close view of the suspended plate above the waveguide is shown in Figure 6.2(b).

The basic principle of operation of hybrid integrated mechano-optical modulator is based on the IONM effect [9]. In the IONM effect, the mechano-optical interaction is achieved by moving an element into the evanescent field of the waveguide mode. The element could change either the real part or the imaginary part of the refractive index. In this study, a metal coated suspended beam is used to introduce loss in the propagation path.

Using a bi-directional electrostatic actuation mechanism, the suspended mechanical beam can be moved towards and away from the optical waveguide. To enable electrostatic actuation between the mechanical element and the optical waveguide, the electrodes beside the waveguide core (see top view of optical chip in Figure 6.1 (a)) are used. Further, to enable the electrostatic actuation between the mechanical element and the anchored substrate, a highly conductive silicon substrate is used in the fabrication of mechanical chip. This allows the movement of the suspended mechanical beam away from the waveguide core by applying a voltage potential between the mechanical beam and the anchored substrate. Thus resulting a bi-directional electrostatic actuation.

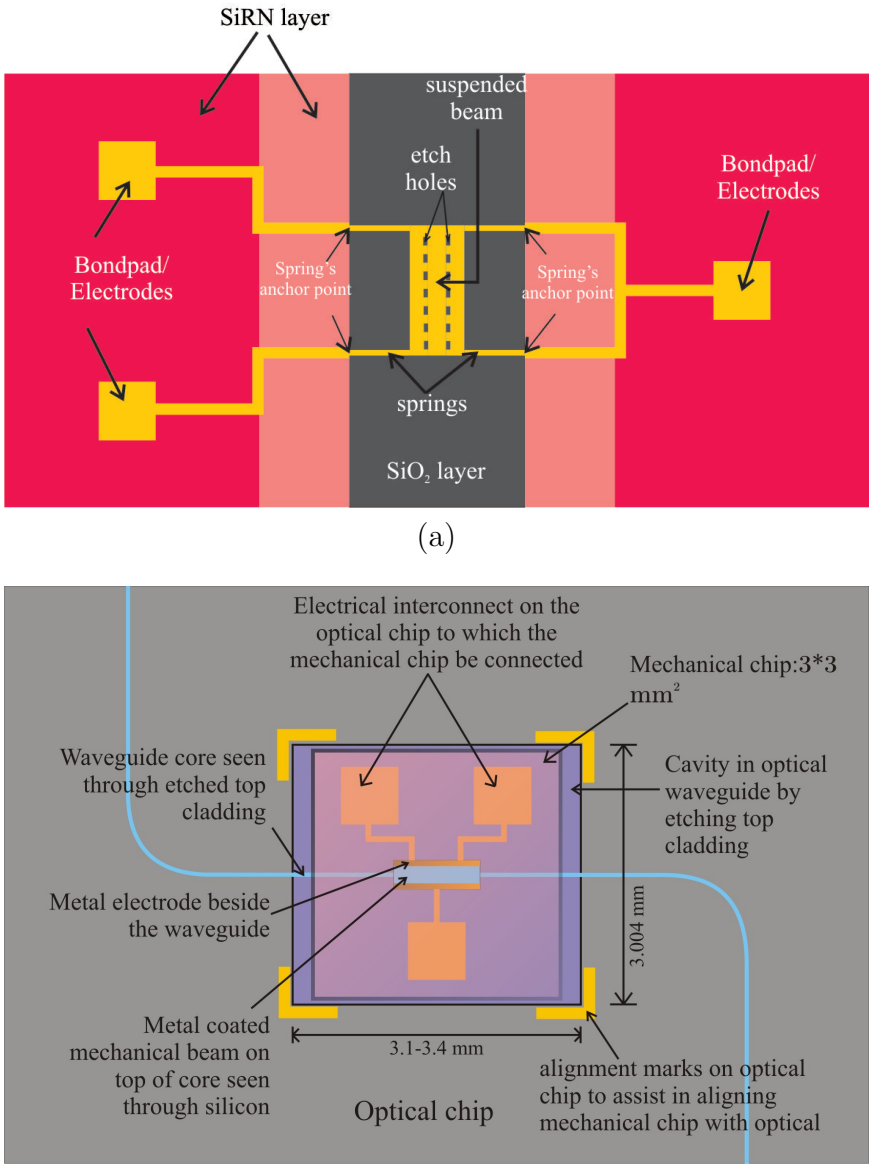


Figure 6.1: Schematic drawings showing top views of (a) Mechanical structure and (b) Optical waveguide chip

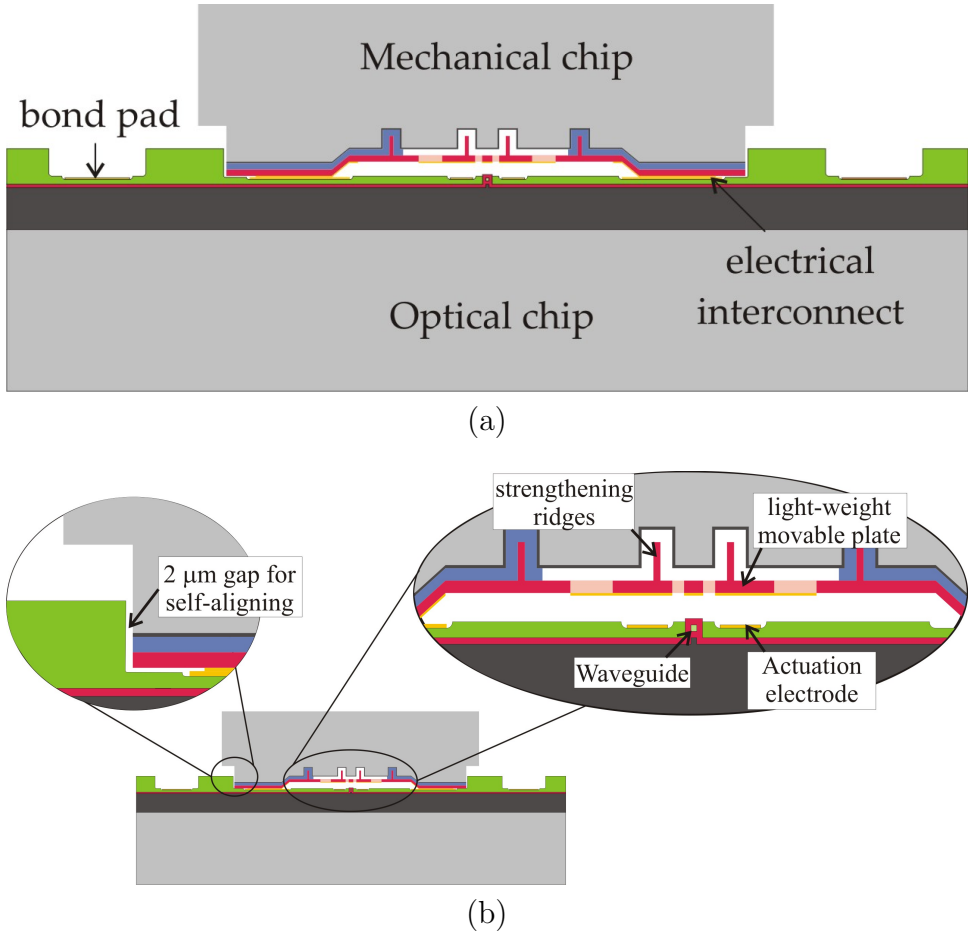


Figure 6.2: (a) Cross-sectional view of the optical modulator design (b) Close-view of the suspended plate structure above the TriPleX waveguide

6.2.1 Optical Waveguide Design

Figure 6.3 shows a schematic top view of the optical chip containing the waveguide. The two key aspects in the optical waveguide chip design are:

- The waveguide is designed with bends in its propagation path in order to assist in confirming whether the incident light at the input port is propagated through the waveguide, which is detected at the output port (see Figure 6.3).
- Anti-stiction bumps are included in the metal electrodes beside the waveguide core, which prevent the beam touching the waveguide core and thereby avoiding any damage. It also helps in preventing any short circuit between the mechanical beam and the metal electrodes beside the waveguide when operated at pull-in occurs.

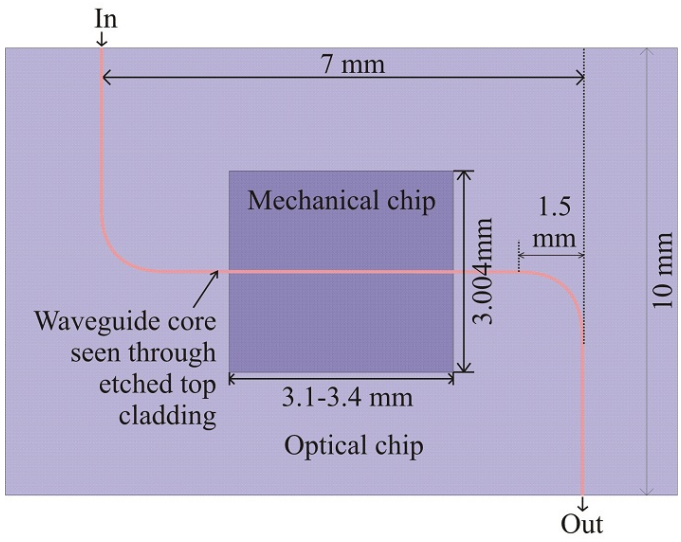


Figure 6.3: Schematic drawing showing the dimensions of the waveguide design-top view

A close view of the optical waveguide chip showing the metal electrode with anti-stiction bumps is shown in Figure 6.4. The width of these bumps is kept similar to that of the waveguide core, and the number of bumps varies according to the length of the suspended mechanical beam. During fabrication of the optical waveguide, care must be taken that no metal is left on top of these anti-stiction bumps.

The area shown as 3x3 mm^2 is where the mechanical chip is mounted. As mentioned before, the mechanical chip is fabricated separately and is self aligned to the optical

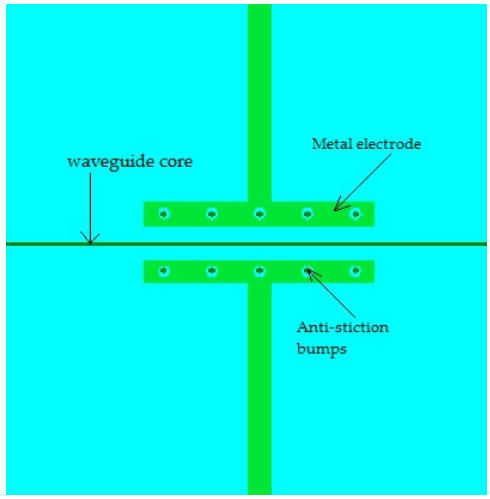


Figure 6.4: Schematic drawing showing the metal electrodes with anti-stiction bumps on the waveguide chip

chip through the cavity (3 x 3 mm^2) formed by etching the top cladding of the optical waveguide. The optical waveguide is designed using TripleX technology developed by LioniX BV [10], for the infra-red wavelength, λ=1550 nm and TE polarization of the propagating mode. TripleX waveguide is a multi layer waveguide (MLW) consisting of vertically oriented high-index contrast layers, which adds more interesting features to the MLWs [10-12]. These waveguides are comprised of a composite core which is made of a thin high-index Si_3N_4 layer encapsulating a low-index SiO_2 inner material. Apart from improving the optical characteristics of the waveguide, the cost to make waveguides and optical devices with the TripleX technology is also significantly reduced. Further, the fabrication process is based on CMOS compatible low pressure chemical vapour deposition (LPCVD) processing.

The cross sections of two possible geometries with the TripleX waveguides are shown in Figure 6.5. In both the cross sections, the confinement of the quasi-TE mode is along the horizontal layer and the quasi-TM mode by the vertical layers. The main advantage of the box shape waveguide is the confinement of the quasi-TM mode due to the high-index vertical layers and a fine tuning of modal birefringence from almost zero to large values. With the box shape and A-shape cross sections, the losses due to birefringence, polarisation and bending are significantly reduced when compared to conventional and high-index contrast waveguides [10].

(a) (b)

Figure 6.5: Cross sections of (a) Box shape, (b) A-shape TripleX waveguides

The design rules for both the box-shape and A-shape waveguides are similar. In our case, A-shape waveguide is chosen, which can be easily fabricated compared to box-shape. The additional slab structure which makes the A-shape also provides additional freedom for the manipulation of waveguide properties.

6.2.2 Concept Validation and Optimisation of Optical Waveguide

The principle of introducing loss in the path of light using a metal coated beam is theoretically verified using the Field designer tool developed by PhoeniX BV [13]. Further, the optical waveguide design is also carried out using the same tool, in which the mode fields are studied, which plays a vital role in determining the confinement of optical energy (mode) within the core. In this section, the optimisation of optical waveguide design and the principle of loss mechanism due to metal layer are explained in detail.

An Optical waveguide is the fundamental element that interconnects various devices in integrated optical circuits similar to what a metal wire does in an electrical circuit. Unlike the way the electrical current that flows through a metal conductor, optical signal travels in different optical modes. The number of modes an optical waveguide can support depends on its cross section, which is determined by the thickness & width of core and cladding layers. Based on that, an optical waveguide can be classified in two broad categories:

- Single mode waveguides
- Multimode waveguides

In both the cases, the propagation depends on the cross section of the waveguide, where any flaw in the cross section introduces loss before the signal is being allowed to propagate. Using Field Designer mode solver tool, the cross section of waveguide is analysed and optimized by studying the mode fields.

With this tool, the optimization of cross section of waveguide by extracting the waveguide modes is performed. It uses film mode matching and finite difference methods to extract the modes [14]. Different analyses are performed for the estimation of various design parameters such as:

- Loss due to movable metal plate
- Loss due to high refractive index substrate
- Bending loss
- Offset value between straight and bend waveguides

From these results, the optical waveguide design is optimized for the Ashape cross section TripleX waveguide. The simulation results are described briefly in the following sub-sections.

Loss due to Movable Metal Plate

The mechano-optical modulator chip is comprised of a mechanical chip bonded to the optical waveguide chip. The modulator prior to any external actuation remains in ON state. The main design parameter here is the required air gap distance between the optical waveguide and the mechanical chip to have loss free propagation of optical signal in its ON state. To extract the optimal air gap value, the mode fields of the optical waveguide are studied for the varying air gap distance between the optical waveguide and the suspended metal layer.

The cross section of A-shape TripleX waveguide with a suspended metal plate above is shown in Figure 6.6. The design parameters used in the analyses are given in Table 6.1. For the air gap analysis, the air gap is varied between the metal plate and the optical waveguide and the corresponding mode fields are studied. The mode fields for different air gap are shown in Figure 6.7, from which it is inferred by moving a metal plate into the vicinity of optical waveguide introduces loss in the path of propagation.

For the initial mode field analysis, gold (Au) is used as the perturbing layer on top of waveguide and air gap between the metal plate and the optical waveguide is varied. The

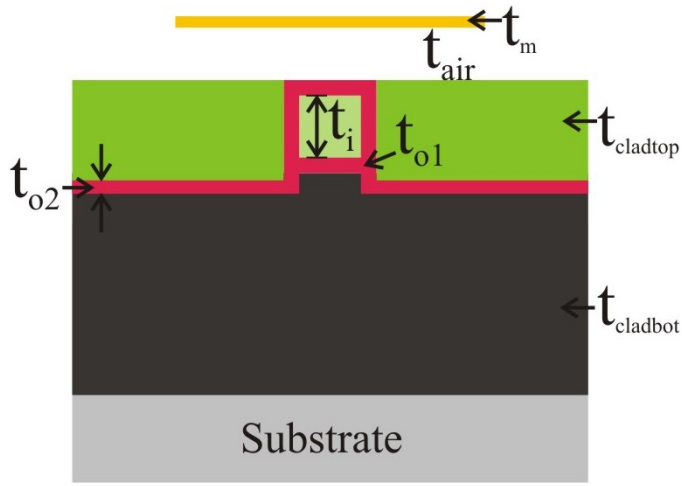


Figure 6.6: Cross section of A-shape TripleX waveguide showing the dimensions

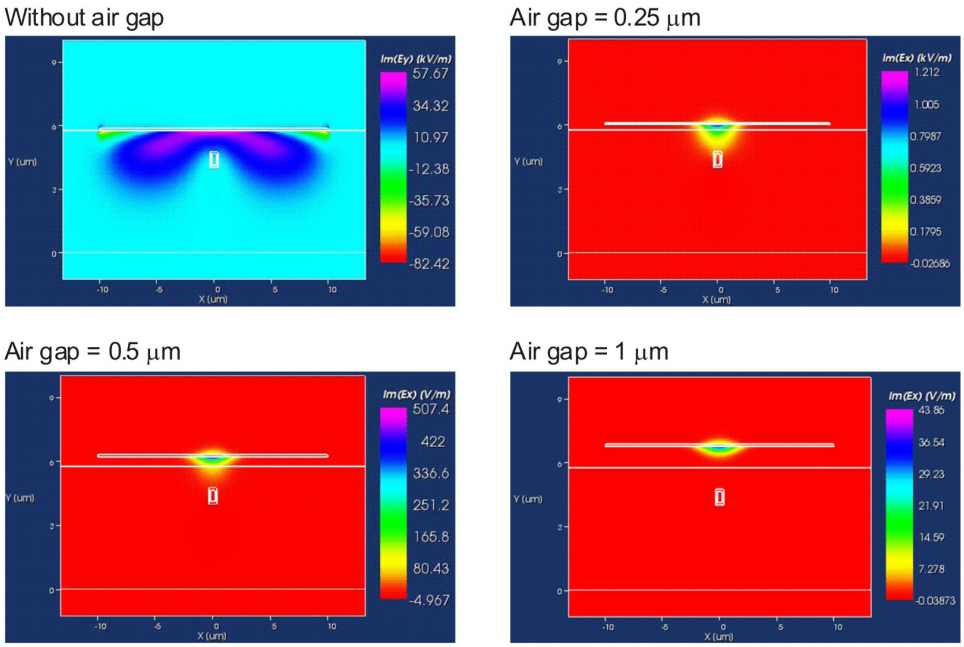


Figure 6.7: Field Designer simulations showing a cross section of the mode field intensities for different air gaps between the waveguide and a suspended metal plate

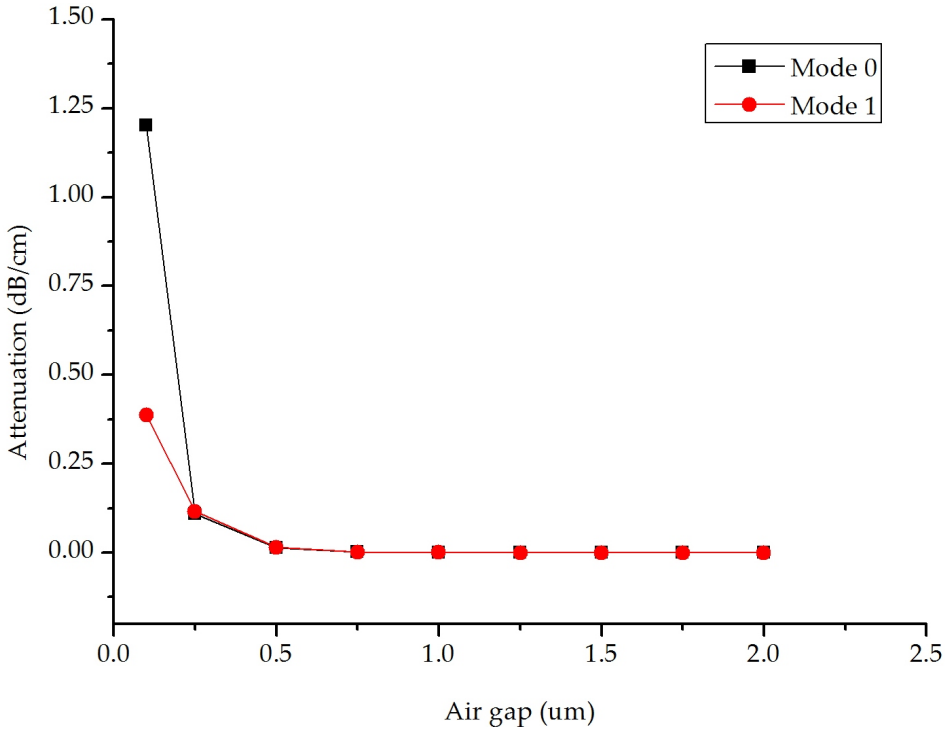


Figure 6.8: Graph showing loss due to metal with varying air gap width

Table 6.1: Dimension of A-shape TripleX optical waveguide used in Field Designer Simulations

Parameter	Dimensions (μm)
$t_{cladbot}$	8
t_{o1}	0.150
t_i	1
t_{o2}	0.150
$t_{cladtop}$	1
t_{air}	0-2
t_m	0.110

loss introduced is a combination of absorption and scattering loss. For a better perceptive, the optical loss due to metal with varying air gap is plotted, and is shown in Figure 6.8. Based on these results, the devices are fabricated with gold for both the electrodes and on the suspended SiRN beam for modulation.

Loss due to High-Index Substrate

The refractive index of substrate plays a vital role in determining the amount of optical power that is being confined in the core region. The refractive index of the silicon substrate is 3.65 at 1.55 μm, which is rather high compared to waveguide materials used. In order to have low optical loss due to high refractive index substrate, an analysis with varying lower cladding thickness was carried out. To have minimal loss towards substrate, the oxide layer (lower cladding) thickness should be at least 4 μm. In fact, this was the first analysis that was performed and an optimal cladding thickness of 8 μm was used in all further analyses and realized devices.

Loss due to Bend

As mentioned earlier, the bending is introduced in order to ensure that the light is being propagated throughout the waveguide. But the inclusion of bend in the path of the light propagation introduces additional loss which needs to be minimized by optimizing the bend radius. Moreover, minimum allowable radius of curvature of the waveguide is mainly dependent on the radiation losses rather than by fabrication tolerances.

In a bent waveguide, modes are hardly bound within the core. And almost all the rays are leaky and radiate power through the mechanisms of tunnelling and refraction [15]. In other words, the total internal reflection in straight waveguide becomes frustrated in a bent waveguide. To visualise this, the mode field of the bent waveguide is analyzed in field designer for its cross section.

The screenshot in Figure 6.9 shows that in the cross-section of a bent waveguide with bending radius R = 50 um, the mode field shifts from the centre of the core to the right. From this shift in the mode field in the bent cross section, it is also inferred that when the cladding layer is thin, the mode field will interfere with the adjacent waveguide mode field, and hence this shift should be less in order to reduce further repercussion.

Further analyses are done with varying bend radius to get the optimal value in order to have minimum bending loss. The mode field analyses shows that the loss due to bend decreases as the bending radius increases, which is shown in Figure 6.10.

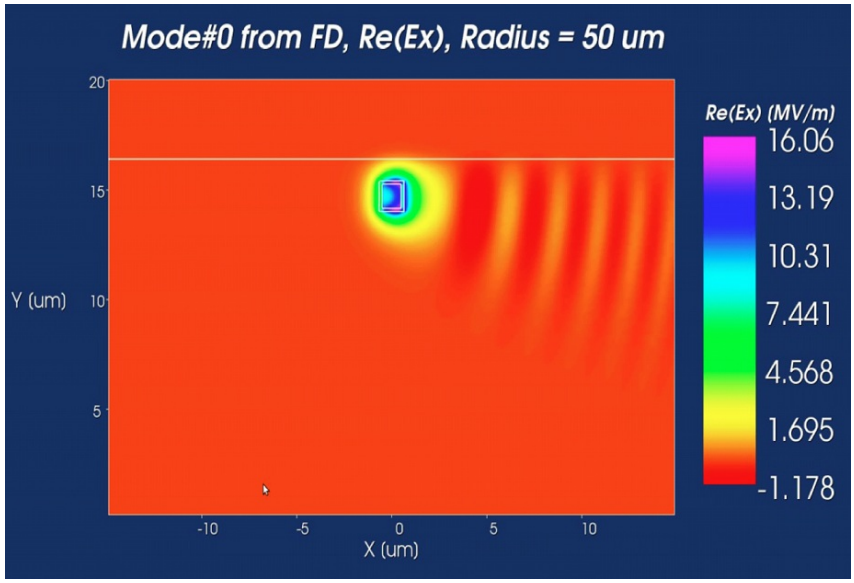


Figure 6.9: Field Designer calculation on a bent waveguide with bending radius of R=50 μm

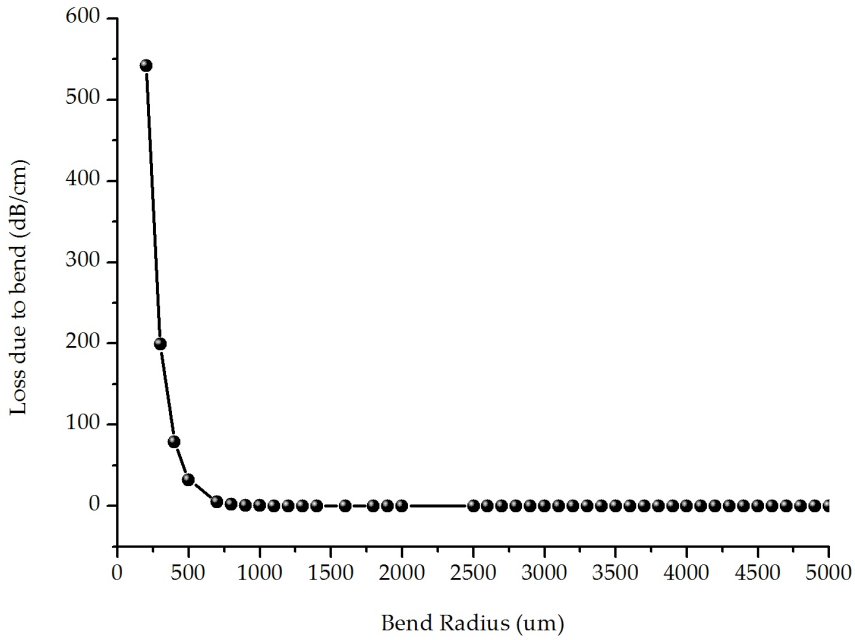


Figure 6.10: Decreasing loss due to bend with increasing bending radius

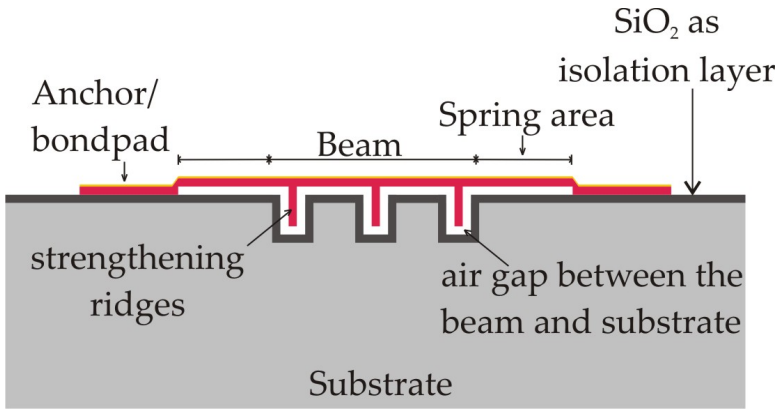
Another factor to be considered is the offset value while connecting the straight waveguide with the bent one. In a bent waveguide, the mode always shifts to the outer edge of the corner and hence it has to be brought back into the straight waveguide that is connected at either side of the bend. The offset values are also calculated for the corresponding bend radii and are used in the design to connect the bend to straight waveguide. The bend radius which has maximum overlap when connected with the straight waveguide is chosen for the waveguide design. For our optical chip design, the bend radius is chosen higher than 1000 μm so as to have good over lap between the straight waveguide and the bend waveguide. The three different bend radii are used in the design are: R = 1000 μm, 2000 μm and 3000 μm.

6.2.3 Modelling of Suspended Mechanical Plate

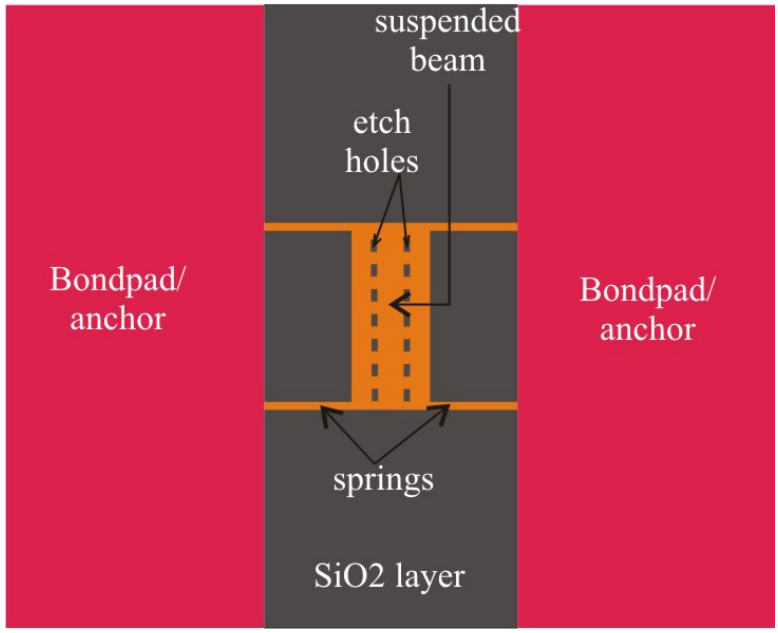
The suspended mechanical element could be of any type such as cantilever, bridge or a membrane. Since the prime requirement is to realise a light-weight mechanical element, focus is given on free-free beam anchored to the substrate through thin springs. Further, these structures are actuated through electrostatic actuation. Figure 6.11 shows a cross sectional drawing and a top view drawing of the suspended mechanical beam.

To enable the actuation between the mechanical element and the anchored substrate, a highly conductive substrate is used for the mechanical design and fabrication. Ultimately, bi-directional electrostatic actuation is performed with the help of the additional electrodes beside the waveguide as shown in Figure 6.1(b). One important characteristic of the electrostatic actuation between parallel plates is its non-linear response which causes pull-in effect. This unstable pull-in effect is used in this study to enhance the switching mechanism.

The suspended beam shown is made of low-stress silicon-rich silicon nitride (SiRN) with a thin layer of gold for actuation and to introduce absorption loss. One of the outcomes of the metal and dielectric layers deposition is the curling of the beam due to the stress gradient or the thermal mismatch induced stress between the layers. To prevent this inherent curling, the beam is strengthened by silicon nitride ridges underneath it. The silicon dioxide layer between the highly conductive substrate and the beam acts as the isolation to prevent the short circuit. The formation of these ridges is explained in the fabrication section that follows later in Chapter 7 of this thesis. The design analysis of the mechanical beam to estimate the resonance frequency and pull-in voltage are carried out using Matlab programming tool. The following sections describe the design equation



(a)



(b)

Figure 6.11: Schematic drawings of suspended mechanical beam, (a) Cross section, (b) Top view

that are utilised in the analyses.

Dynamic Modelling of Mechanical Beam

The purpose of the IONM based approach is to have fast responding switch through mechanical perturbation. In such cases, the switching speed solely depends on the dynamic response of the mechanical beam. This can be achieved by designing light-weight beams since lighter the mass, faster is the movement of the beam, which is simply inferred from the fundamental resonance frequency equation of the beam and is given by:

$$f = \frac{1}{2\pi}\sqrt{\frac{K}{m}} \tag{6.1}$$

The frequency response of beam is useful in determining the switching time of the mechanical switch, the mechanical bandwidth over which it can be used and the effect of thermal noise. In the current study, the main requirement is the switching speed in the order of 1 μs to modulate the optical signal, for which an analytical approach to show the feasibility of achieving 1 μs as switching time is performed. The analysis started with the fundamental dynamic equation of motion of a suspended plate, given as:

$$m\frac{d^2x}{dt^2} = -K(x - x_0) - D\frac{dx}{dt} + F_{el} \tag{6.2}$$

where m is the mass of the plate, K is the spring constant of the suspension spring and D is the damping constant. For a parallel plate configuration with plate separation, x and area A, the electrostatic force, F_{el} as a function of voltage V is given by:

$$F_{el} = \frac{\epsilon_0 A V^2}{x^2} \tag{6.3}$$

To compute the switching time analytically, the initial conditions applied are: $x = 0$ and $dx/dt = 0$ at $t = 0$ (switch is at rest), and the switching time is calculated for the condition, $x_0 = x$ and is given by [14, 15]:

$$t_s = 3.67\frac{V_p}{V_a\omega_0} \tag{6.4}$$

where V_p is the pull-in voltage, which has been discussed in the following section, $\omega_0 = \sqrt{K/m}$ is the mechanical resonant frequency as described in Equation 6.1 and V_a is the applied voltage. For damping dominated system, considering constant damping with gap

height and neglecting the acceleration and spring component, the equation of motion becomes:

$$D\frac{dx}{dt} = F_{el} \tag{6.5}$$

Equation 6.5 can be solved with integral methods or difference methods. The solution using integral method and applying Equation 6.3 for F_{el}, results in

$$t_s = \frac{2Dx^3}{3\epsilon_0 A V_a^2} \approx \frac{9V_p^2}{4\omega_0 Q V_a^2}, \text{for} \qquad V_a > V_p \tag{6.6}$$

Further estimation assuming constant F_{el} and a constant velocity approximation ($dx/dt = x/t_s$) leads to the following equation, which is again for $V_a > V_p$

$$t_s = \frac{V_p}{\omega_0 V_a}\sqrt{\frac{27}{2}} \tag{6.7}$$

From the Equations 6.4 - 6.7, it is seen that the switching time strongly depends on the applied voltage, since the larger the voltage; the stronger is the electrostatic forces. Switching time as a function of applied voltage for different ω_0 (of 3 different beam length, 250 μm, 125 μm and 65 μm) is shown in Figure 6.12, from which, it is inferred that to obtain switching time in the order of μs, applied voltage should be in the order of 50 to 60V.

The characterisation and operation of the MEMS devices are mainly done at atmospheric pressure. Under these conditions, the quality factor is usually dominated by squeeze film damping ($Q = K/(\omega_0 D)$). The quality factor is determined by several different variables such as pressure, temperature and intrinsic material dissipation. For a damping-limited device, the switching time estimation using Equation 6.7 tends to over estimate the switching time whereas Equation 6.6 underestimates its value.

The switching time estimation shown above is based on the second order system/device response techniques; this is because upon removal of actuation voltage V_a, the system behaves like a second order system. In such cases, the non-linearity introduced by the squeeze film damping should also be taken care of. The primary way to estimate the response of a system is by determining the damping of the system, whether it is under damped, over damped or critically damped.

For this device, the damping will be dominated by the squeeze film effects of the air trapped between the beam and the substrate. A rough estimate of the damping resulting

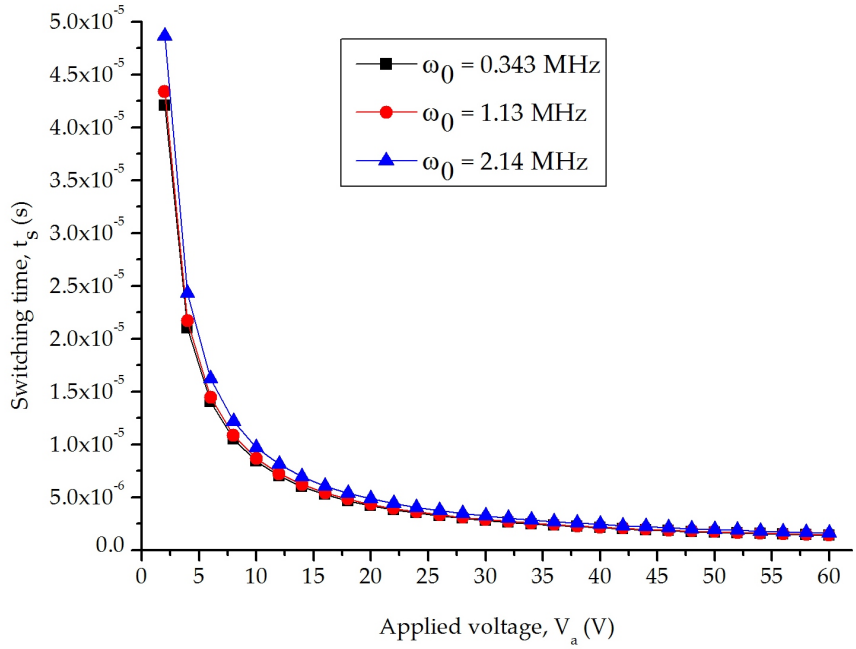


Figure 6.12: Switching time calculated as a function of applied voltage for different mechanical resonant frequency, ω_0

from squeeze film effect is found in [14], and the damping constant is given by:

$$D = \frac{3}{2\pi}\frac{\mu A^2}{x^3} \tag{6.8}$$

where μ is the viscosity of the fluid, A is the area of the beam, and x is the air gap beneath the beam. From this equation, it is seen that the damping is strongly dependent on the air gap x. One way to reduce this effect is to have holes on the beam. This is discussed in Section 2.4 that follows later in this chapter.

Equation 6.8 is derived for small displacements or bending of the beam, where as this is not the case when the beam is pulled down to the lower electrode or when it releases. Therefore this should be always treated as the rough estimation of the beam behaviour. In practical case, the damping behaves in a non-linear fashion for which the computational fluid techniques are required to analyse for larger displacements.

Quasi- Static Modelling of Mechanical Beam

Because of the non-linear behaviour of the Equation 6.2, quasi-static conditions ($\frac{d^2x}{dt^2} \approx \frac{dx}{dt} \approx 0$) are always assumed for simplification, which gives:

$$Kx_0 = \frac{\epsilon_0 A V_a^2}{2(x - x_0)^2} = F_{el} \tag{6.9}$$

where K is the spring constant, and V_a is the applied voltage. The spring constant, K is given by [18]:

$$K = 16 E w_s \left(\frac{t}{l_s}\right)^3 \tag{6.10}$$

where w_s is the width of the spring, t is the thickness and l_s is the length of the spring. The product $Ew_s(t/l_s)^3$ is the flexural rigidity which accounts for the material property (E) and the moment of inertia ($I = w_s(t/l_s)^3$). Solving Equation 6.11 for applied voltage gives us:

$$V_a = \sqrt{\frac{2Kx_0}{\epsilon_0 A}}(x - x_0) \tag{6.11}$$

In the whole domain ($0 < x_0 < x$), Equation 6.11 has a maximum that occurs at $x_0 = 2x/3$. This happens as the increase in the electrostatic force is no longer compensated by the restoring spring force, resulting in the instability of the beam position and eventually the collapse of the beam over the lower electrode. This is referred to as pull-in and the corresponding voltage is called pull-in voltage, V_p, which can be obtained as:

$$V_p = V\left(\frac{2}{3}x\right) = \sqrt{\frac{8Kx^3}{27\epsilon_0 A}} \tag{6.12}$$

Beyond pull-in voltage, application of higher voltage leads to experience the bifurcation to an equilibrium point located at $x_0 > x$, which in reality can not be fully realised due to the fixed electrode. Instead, the moving electrode falls onto the fixed electrode and is held by it, which is unavoidable. In our case, to avoid this permanent stiction caused by pull-in, we have included ridges underneath the beam, which also helps to keep it flat. Figure 6.13 illustrates the pull-in bifurcation as observed in the parallel plate electrostatic actuator. The pull-in value shown here is for a beam of dimension: length, $L_b = 125$ μm, width, $w_b = 40$ μm and thickness, t = 1μm. In designing the parallel plate actuator, the main design parameters that are varied are the spring stiffness K and the area of the beam, by keeping the initial distance x a fixed parameter.

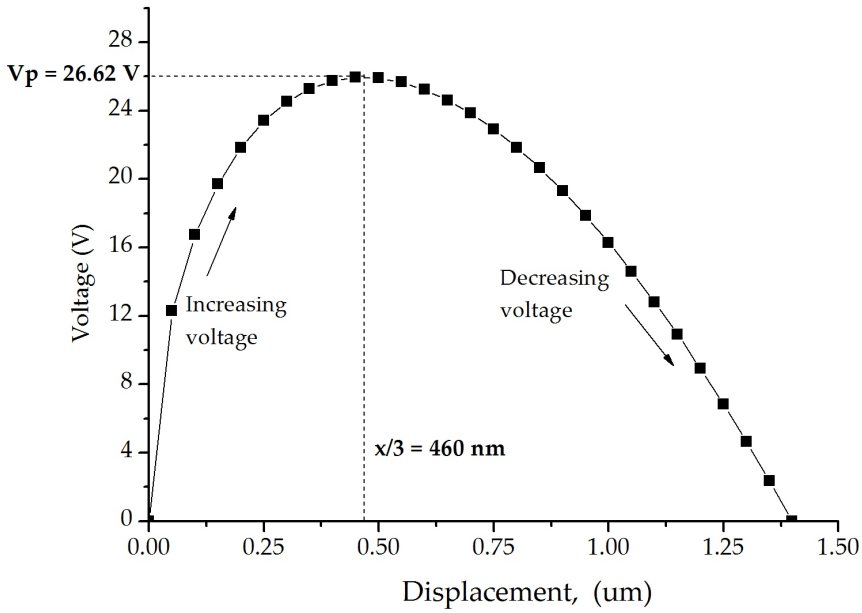


Figure 6.13: Quasi-static equilibrium curve for parallel plate actuator based on Equations 6.11 and 6.12

6.3 Final Design of Mechanical Chip to Integrate with Optical Chip

The analyses to realise the suspended mechanical beam is carried out using Matlab [19]. The prime requirement of mechano-optical modulator research is to have fast switching mechanical element, for which the design is mainly focussed on achieving 1 μs as switching time. Figure 6.14 shows the switching time estimation using Matlab/Simulink with realistic values for the parameters: mass m = 2 x 10^{-11} kg, spring stiffness K = 5 N/m, damping constant D = 1x 10^{-5} N/(m/s) and air gap x_0 = 1 μm. A short, 65 V pulse is used to get the plate moving. The voltage is reduced to a few volts just before the plate's collapse, which is sufficient to keep the movable plate pulled-in. It is evident from the analysis that a light weight movable plate can introduce ON/OFF switching of optical signal in just 1 μs.

The response of beam to an applied voltage is rather complex in nature due to several reasons. For example, the stepped up anchors used in the design of the beam do not typically match with the analytical design. The etch holes in the beam also creates more complex mechanical and electrostatic response than the solid beam. Finally, the effect of

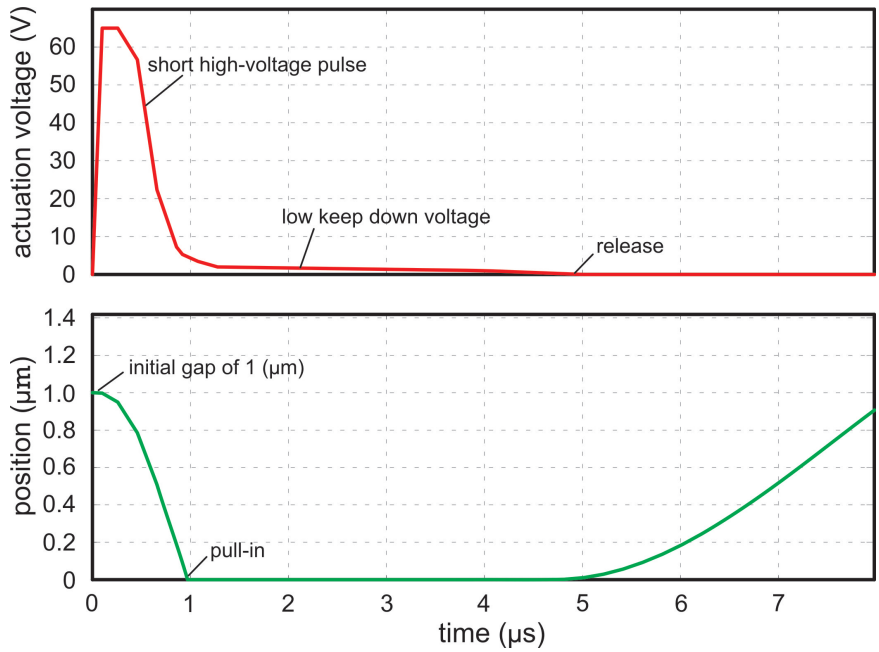


Figure 6.14: Switching time estimation using Matlab/ Simulink

residual stress in the beam also plays a vital role. To analyse all these effects, one way of modelling is to use finite element method, which takes into account at least the effects of etch holes, stress etc.

The beam is therefore modelled using both analytical calculations and FEM simulations using Intellisense tool [20]. In both analyses and simulations, the thickness of the beam is kept constant, the length and width of the beam are varied. A schematic representation of the mechanical beam studied analytically and using FEM simulations is shown in Figure 6.15 and the dimensions of the beam and spring are given in Table 6.2. The material properties used in the design analyses are given in Table 6.3. The results of analytical calculations and FEM simulations for the mechanical structure shown in Figure 6.13 with different beam lengths are given in Table 6.4. The measured results of the same are discussed later in this thesis in Chapter 6 & 7 that can be compared with the analytical calculations and FEM simulations.

Initially, mechanical test structures based on the analytical model presented in earlier sections were designed. These structures were fabricated and characterised for the pull-in voltage and resonance frequency measurements. Based on the results from the fabrication and characterisation, the optimum spring design and beam dimensions to achieve fast

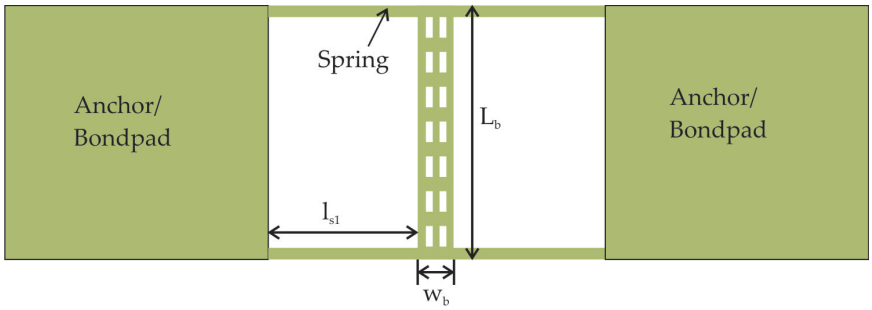


Figure 6.15: Schematic representation of suspended mechanical beam

Table 6.2: Dimensions of the mechanical beam and the spring structure used in the analyses and simulation

Parameter	Values (μm)
Length of beam, L_b	65 to 250
Width of beam, w_b	35
Thickness of beam, t	1
Length of spring, l_{s1}	100
Width of spring, w_s	10
Thickness of spring, t	1

Table 6.3: Material properties of the mechanical beam

Parameter	Values
Young's modulus of SiN, E_1 (GPa)	276
Young's modulus of Au, E_2 (GPa)	78
Density of SiN, ρ_1 (Kg/m^3)	2887
Density of Au, ρ_2 (Kg/m^3)	19320
Permittivity of free space, ϵ_0 (F/m)	8.854x10^{-12}

Table 6.4: Estimated results from analytical calculations and FEM simulations with measured values

Property	Length of beam	Width	FEM results	Analytical results	Measured
Units	μm	μm	kHz	(MatLab) in kHz	kHz
	350	35	56.00	63.01	44.625
Resonance	250	35	69.54	73.6	54
frequency	125	40	237.60	225.9	186.274
(kHz)	80	40	326.26	304.66	297
	65	35	421.86	386.59	340.25
Units	μm	μm	V	(MatLab) in V	V
	350	35	-	6.31	-
Pull-in	250	35	25.57	17.9	25
Voltage	125	40	-	26.40	24
(V)	80	40	-	46.47	-
	65	35	-	56.65	-

switching speed in the order of μs are chosen. The fabrication schemes for the test structures and ultimately the mechanical chip to integrate with the optical chip are presented in Chapter 7.

In the mechanical beam design, the number of strengthening ridges underneath the beam depends on the width of the beam. In the test structures fabrication, the number of ridges used beneath the beam is in the order of 2-3 depending on the width of the beam. One important factor need to be taken care with the ridges is that the beam area that comes above the waveguide core of 1 μm width should remain flat. From the fabrication results presented in Chapter 7, it is observed that the beam has a curved (inwardly) shape wherever it has ridges, and hence it doesnt remain flat over the area having ridges (see Figure 7.4). Therefore it is recommended not to have ridge beneath the beam area which overlaps with the optical core to perform modulation. For which the number of ridges is chosen to be 2 with two different beam widths such as 35 μm and 40 μm.

Further, from the resonance frequency and pull-in voltage measurements, the optimum length of the beam to achieve high switching speed is chosen to be in the range of 50 to 125 μm. Eventually, in the integrated mechano-optical modulator chip, the mechanical beam is presumed to be suspended in a lengthwise direction with the optical waveguide; that

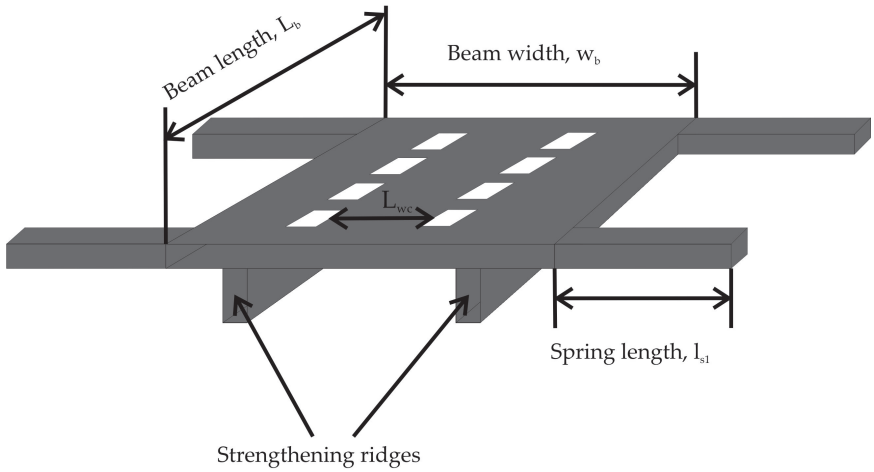


Figure 6.16: 3D drawing of suspended mechanical beam showing the dimensional parameters

the length of the beam is parallel to the length of the waveguide. A schematic drawing of the suspended mechanical beam with dimensional parameters is shown in Figure 6.16 and the final dimensions of the beam and spring are given in Table 6.5.

6.4 Conclusion

In this Chapter, detailed design analysis of the IONM based optical modulator is described. Using hybrid integration, the mechanical structure is connected to the optical chip to form a mechano-optical modulator. The design of the optical chips, which is based on the TripleX technology and the mechanical chips are individually discussed here. With the TripleX technology, by only acting on the waveguide geometry and without changing the refractive index of the materials, different confinement regimes can be achieved for the specific applications. A-shape geometry is chosen for the optical modulator in order to have ease of fabrication. Using Field designer mode solver tool, the optimisation of the optical waveguide design is carried out. The design of mechanical chip shown here is mainly focussed on realising light weight structure to enable fast mechanical movement.

An important characteristic of the mechanical structure is the inclusion of ridges underneath the beam. These ridges keep the beam flat and also avoid the stiction of the mechanical beam to the substrate when operated at pull-in voltage. This functionality is

Table 6.5: Dimensions of mechanical beam to be integrated with the optical chip

Parameter	Values
Length of beam, L_b (μm)	65 to 125
Width of beam, w_b (μm)	35, 40
Thickness of beam, t (μm)	1
Length of spring, l_{s1} (μm)	100
Width of spring, w_s (μm)	10
Thickness of spring, t (μm)	1
Mechanical beam-core overlap length, L_{wc} (μm)	7
Mass of beam, M (kg)	0.78x10^{-11} to 1.74x10^{-11}
Spring constant, K_s (N/m)	$\sim$40.1

experimentally demonstrated in Chapter 7 and 8. Further, using bi-directional electrostatic actuation, the suspended mechanical beam can be moved towards and away from the waveguide core. This concept too is experimentally demonstrated in Chapter 8. The concept of introducing loss in the optical path using a metal coated beam is analytically verified using Field designer mode solver tool. Gold as metal is used in the analyses, which showed the feasibility of introducing absorption loss in the optical path. Both the mechanical structure and the optical waveguide are realised using fabrication schemes discussed in Chapter 7.

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Chapter 7

Towards a Fast Mechano-Optical Modulator: Device Fabrication

Synopsis

This chapter presents the fabrication of the mechano-optical modulator based on the IONM design principle described in Chapter 6. As the prime focus is on realising the light-weight mechanical element, mechanical test structures were first fabricated. Based on their characterised results, the final design of the mechanical element for the mechano-optical modulator is devised. The fabrication of both the optical waveguide and mechanical element for the hybrid integration are explained in detail. The hybrid integration is made possible with a self-aligned assembly technique solely developed for such integration, which restricts the maximum misalignment error to at most 2 μm.

7.1 Introduction

The mechanical chip which consists of the beam attached to substrate through suspension springs is designed to be fabricated using a combination of both bulk and surface micromachining. To develop insight into the design and fabrication of the beam with strengthening ridges underneath them, a wide range of prototypes of beam structures were designed and fabricated. The prototypes include beams of varying length and width with different spring structures such as serpentine flexure, folded flexure, solid beam (no flexure) and crab-legged flexures. Within each of the spring structure, length of the beam is varied from 50 to 350 μm for three different widths 40 μm, 35 μm and 25 μm. The width of the beam is chosen based on the number of ridges it could have. For example, 40 μm and 35 μm wide beams consist of 3 ridges and 25 μm consist of 2 ridges. Schematic drawings of mechanical beam with different spring structures are shown in Figure 7.1.

7.2 Fabrication of Test Structures of Mechanical Element

The outline of the fabrication process used to realize these test structures is given in Figure 7.2. As the electrostatic actuation is applied between the gold coated SiRN beam and the silicon substrate, the processing is performed on a highly conductive silicon substrate. The process starts with creating trenches on the silicon substrate using reactive ion etching, followed by the oxidation of silicon to get 1 μm thick oxide layer. This oxide layer acts as both the etch stop layer during sacrificial layer etching and also as the isolation between the SiRN beam and the substrate during electrostatic actuation. Next, 1.5 μm of polysilicon is deposited through LPCVD, which acts as the sacrificial layer, and this defines the initial air gap between the released beam and the substrate.

Photolithography is done to pattern the anchor/bond-pad on the polysilicon layer and followed by etching it using reactive ion etching. After removal of the photoresist, 1 μm thick SiRN is deposited using LPCVD, followed by sputtering of thin layers of chromium (Cr, 10 nm) and gold (Au, 100 nm). These three layers are then etched using one mask material (Olin 908-35). Finally XeF_2, which has nearly infinite selectivity to silicon over materials including photoresist, silicon dioxide, silicon nitride and aluminium is used to etch the polysilicon layer and ultimately release the mechanical structures [1, 2].

The photoresist Olin 908-35 can be removed either prior to the release of structures

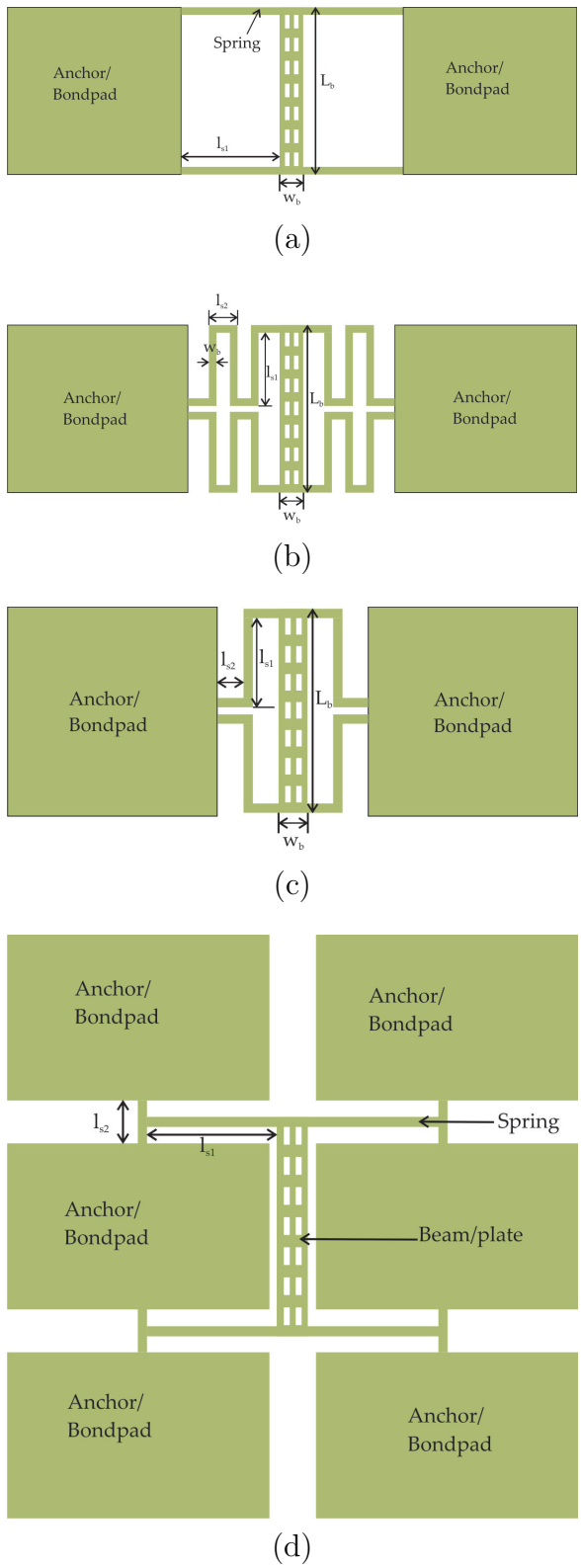


Figure 7.1: Schematic drawing of mechanical beam with (a) Solid beam spring, (b) Serpentine flexure, (c) Folded flexure and (d) Crab-legged flexure

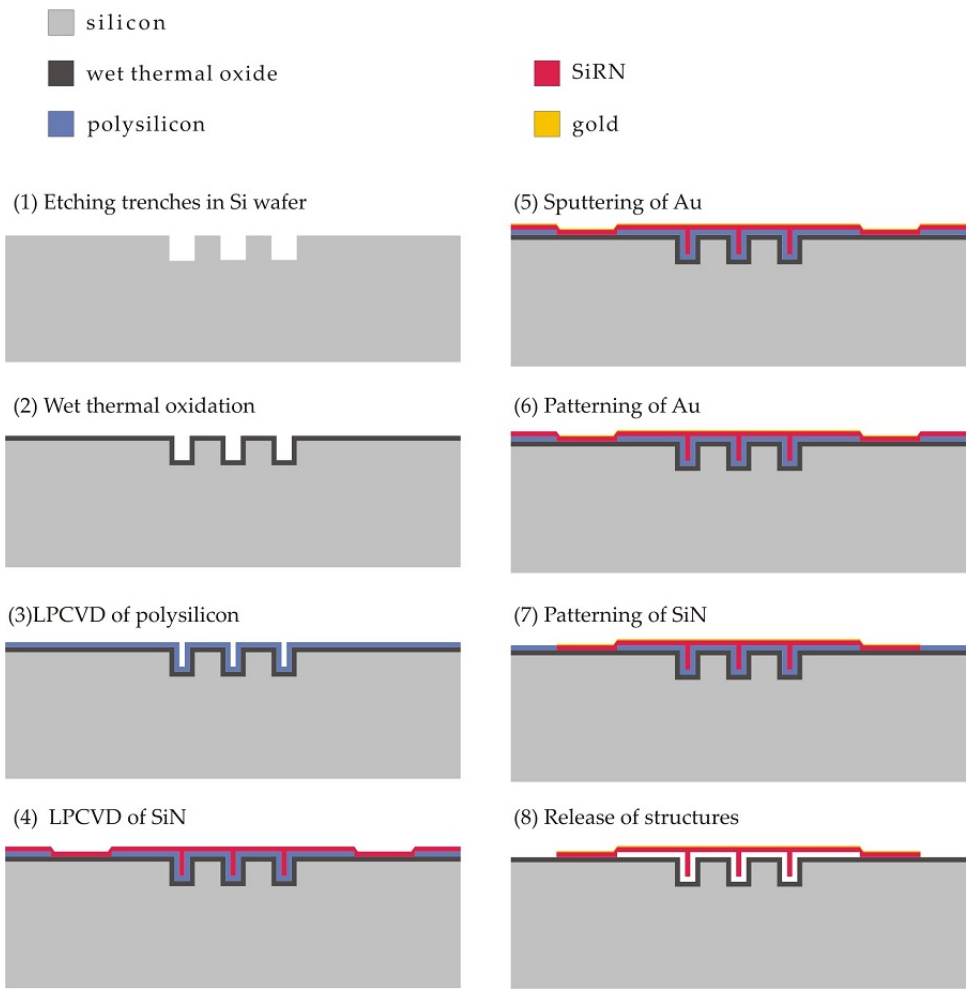
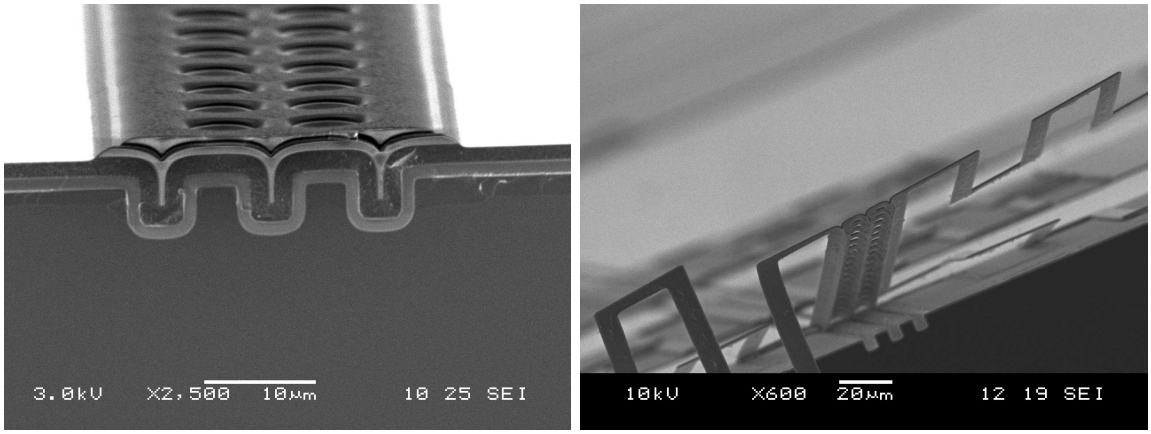


Figure 7.2: Outline of fabrication process for mechanical test structures

in XeF_2 or after the etching. It was observed that when photoresist is removed using O_2 plasma in a barrel etcher, the Cr layer was being attacked and this resulted in the poor adhesion of Au with the beam layer SiRN. Further, after releasing the beams, it is not suitable to use any wet etchant which results in the stiction of beams and springs. Therefore, the optimum way is to remove the resist prior to the release of structures using both O_2 plasma and 100% HNO_3.

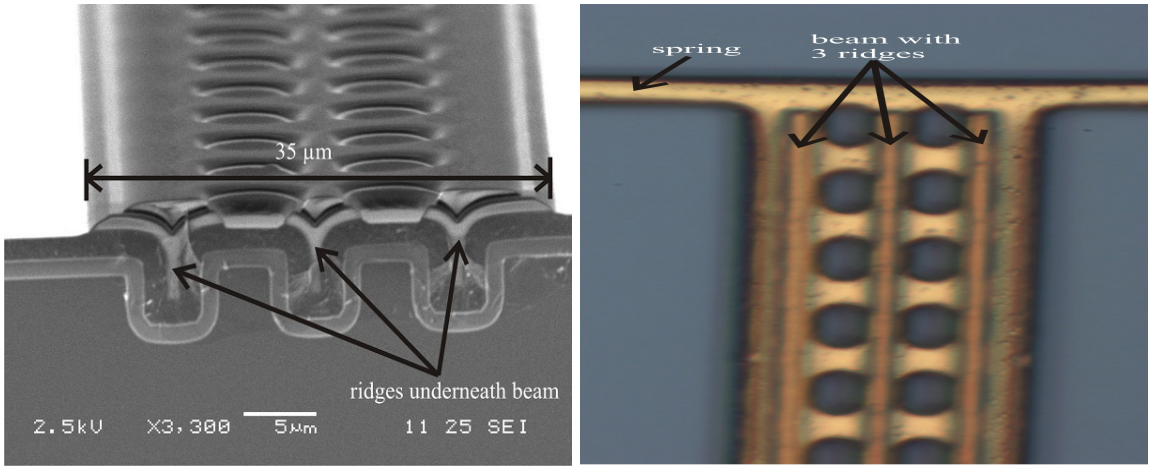
Figure 7.3 shows the SEM image of the realised structure before and after sacrificial layer etching. The silicon substrate was broken in order to be able to look under the device. One of the suspension springs is stuck behind the edge of the substrate, causing the tilting of the device in this case. The photograph clearly illustrates the effectiveness of the strengthening beams: the plate/beam remains flat, even in this situation where the suspension springs have an enormous deflection.



(a) (b)

Figure 7.3: SEM images showing the cross sections of realised beam (a, left) before sacrificial layer etching & (b, right) after sacrificial layer etching

A detailed SEM image and micrograph image of the cross section and top view of the beam (having width of 35 μm) is shown in Figure 7.4. Few beam structures without ridges are also included in the design for a comparative study. Some of the realised test structures with different spring are shown in Figure 7.5. From these test structures the optimised beam length and width with suitable spring structure is selected to be used in the final mechanical beam that can be integrated with the optical chip.



(a) (b)

Figure 7.4: (a) SEM image showing the cross section of beam with ridges, (b) microscope image showing the top view of beam with springs

7.2.1 Trench Dimension Optimisation

The ridges underneath the mechanical beam that are formed in Step 4 are designed to provide additional strength to the beam and also to prevent bending of beam due to any stress gradient. The width and depth of these strengthening ridges depends on the following parameters:

- Width and depth of the trench created in Step 1
- Thickness of oxide, Step 2
- Thickness of polysilicon, Step 3

The oxide and polysilicon thicknesses are to be chosen in such a way that after their deposition, the gap to be filled in by SiRN should be 1 μm. As the stress effects in SiRN structures increase with increasing thickness, it is important not to exceed the SiRN thickness beyond 1.5 μm. Therefore it is important to check the profile of the etched trench and change the thickness of oxide and polysilicon. Three different cases having different widths of the trench is shown in Figure 7.6.

7.2.2 Effect of Holes in the Beam

The designed beam for both the test structures and the final version has holes on its surface, which is mainly included as etch holes to remove the sacrificial layer (polysilicon).

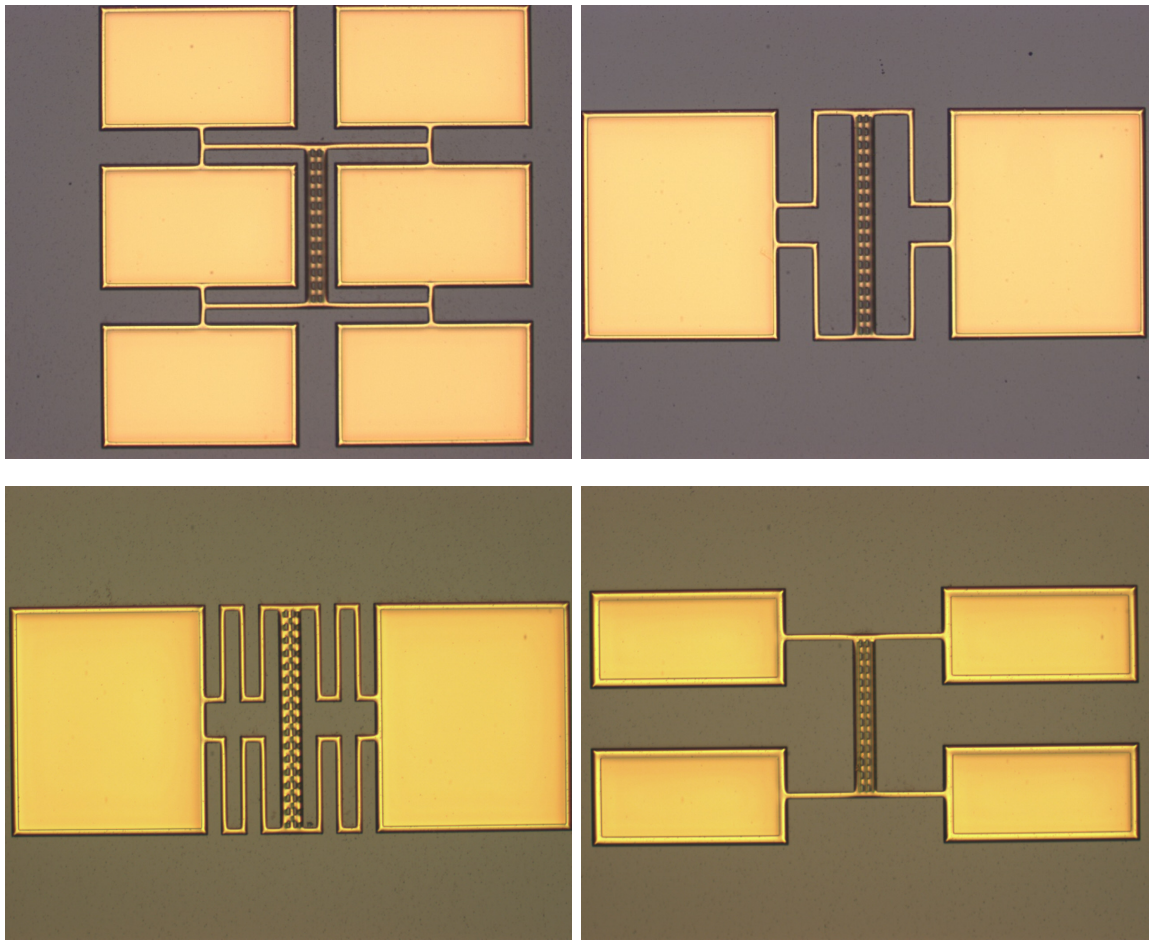


Figure 7.5: Optical micrographs of test structures that were fabricated to evaluate different spring design

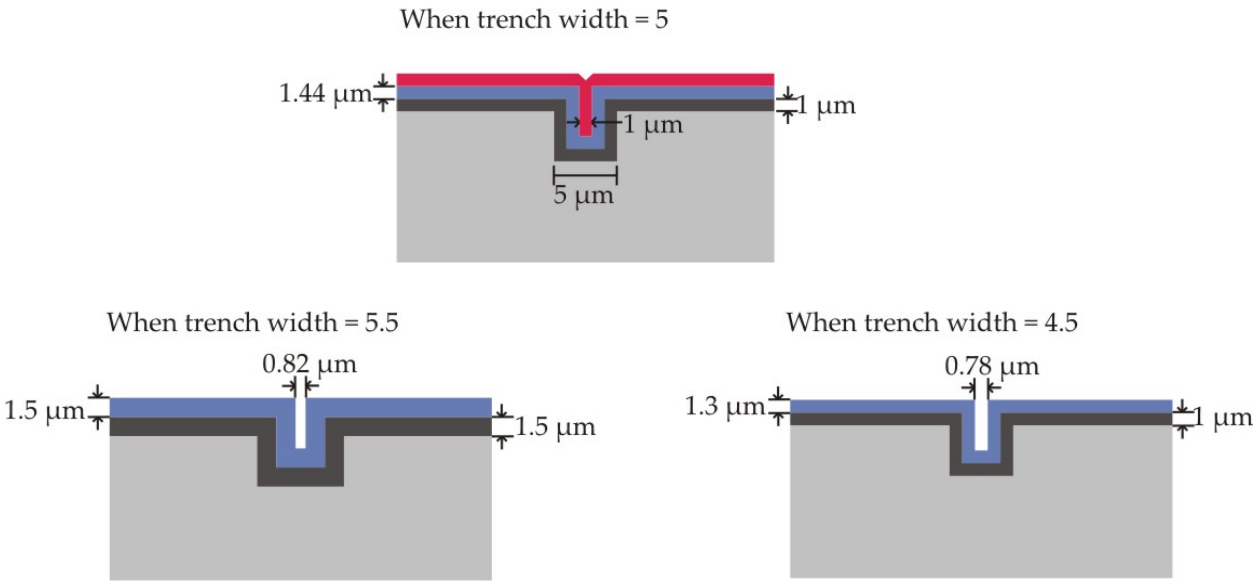


Figure 7.6: Cross section of trenches with varying values of oxide and poly thickness (a) for trench width = 5 µm, (b) & (c) for two different trench widths = 5.5 µm and 4.5 µm

The top view of the beam is shown in Figure 7.7. The etch holes are in the order of 10x3 μm^2 along the beam length. Apart from acting as access holes to etch the sacrificial layer within the trenches, the etch holes in most of the MEMS structures are generally included to reduce the squeeze film damping and increase the switching speed. The hole/perforation area can be up to 60% of the beam surface area. The hole/perforation pattern is characterised by the ligament efficiency which is defined as the ratio of remaining width to the pattern pitch and is given by [3]

$$\mu = \frac{1}{pitch} \tag{7.1}$$

The holes are also known to release some of the residual stress that is inherent in the beam which in turn reduces the Youngs modulus of the beam. The reduction in the residual stress can be given as:

$$\omega = (1 - \mu)\omega_0 \tag{7.2}$$

where ω_0 is the residual stress without holes. The presence of holes also reduces the mass of the beam, which in turn increases the resonance frequency of the beam. The holes also affect the electrostatic force if the size of the hole exceeds as described Reference 3.

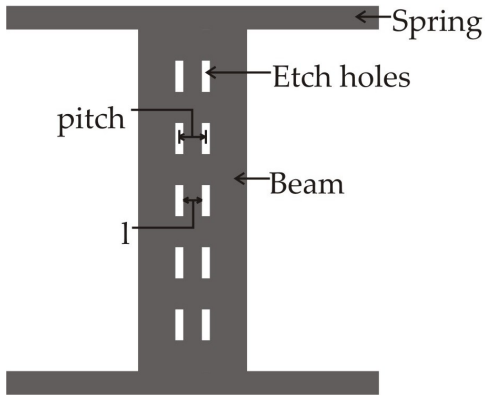


Figure 7.7: Beam showing the etch holes with parameter for the ligament efficiency

The effect is mainly due to the fringing fields that fills the hole's gap in the beam. The effect is negligible if the hole dimension lies in the range of 3-4x (where x is the air distance between the parallel plates).

7.2.3 Characterisation of Test Structures

The realised devices were characterized using a Polytec MSA-400 Micro System Analyser [4]. During analysis and simulations, the strengthening ridges underneath the beam are neglected to avoid complexity in calculations. Presence of these ridges increases the mass; thus the effect could be seen in the resonance frequency measurements. In addition to the ridges, the residual stress in the beam also plays a vital role in static measurements. The static pull-in measurements were carried out at room temperature and ambient pressure using a White Light Interference Microscopy (WLIM, Polytec MSA 400) and the dynamic measurements were performed in Laser Doppler Vibrometry (LDV, Polytec MSA 400). Since the system could be highly affected by the squeeze film damping of the air in between the beam and the substrate, the dynamic measurements were done at atmospheric pressure as well as under vacuum pressure down to 7.3 x 10^{-3} mbar.

7.2.4 Static Pull-in Measurements

Figure 7.8 shows a typical result of pull-in measurement where the suspended plate displacement is plotted as a function of the applied actuation voltage. The pull-in voltage obtained was ∼25 V, which matches approximately with the value obtained by FEM simulation (25.57 V) discussed in Section 6.3 of Chapter 6. Measurement result shown here

was done for the beam of length L_b = 250 μm, width w_b = 35 μm and thickness t = 1 μm having 3 ridges.

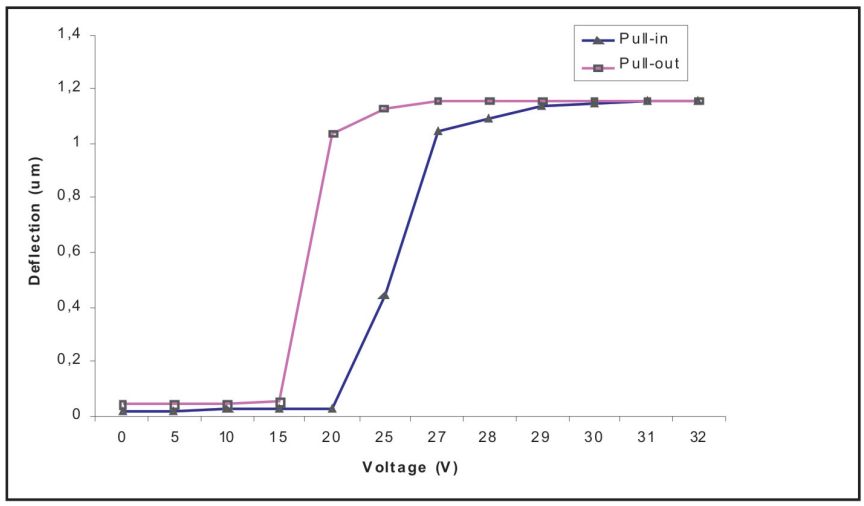


Figure 7.8: Displacement as a function of applied actuation voltage measured using a Polytec MSA-400 Micro System Analyser

The main advantage with these beams is that they do not get stuck to the lower electrode, in our case the highly doped silicon substrate, during pull-in measurement. This is due to the presence of strengthening ridges which reduces the surface area of contact. When the voltage is reduced from the pull-in value, the beam gets back to its original position following a path defined by hysteresis.

7.2.5 Resonance Frequency Measurement

Resonance frequency for different beams with different spring structures was measured in Laser vibrometer. As mentioned previously that the system is highly dominated by the squeeze film damping, the resonance frequency measurements were done both in atmospheric pressure and in a vacuum chamber at a pressure of 8.6 x 10^{-2} mbar. Figure 7.9 shows a typical frequency response as measured from laser vibrometer at chamber pressure of 8.6 x 10^{-2} mbar. The resonance frequency shown here is for the beam having dimensions: length l_b = 250 μm, width w_b = 35 μm having 3 ridges and is measured as 54 KHz. Resonance frequency of mechanical beam having different lengths and widths are also measured and are given in Table 6.4 in Chapter 6.

The characterisation of these test structures is mainly performed to understand the behaviour of different spring designs and hence select the best suitable beam-spring model

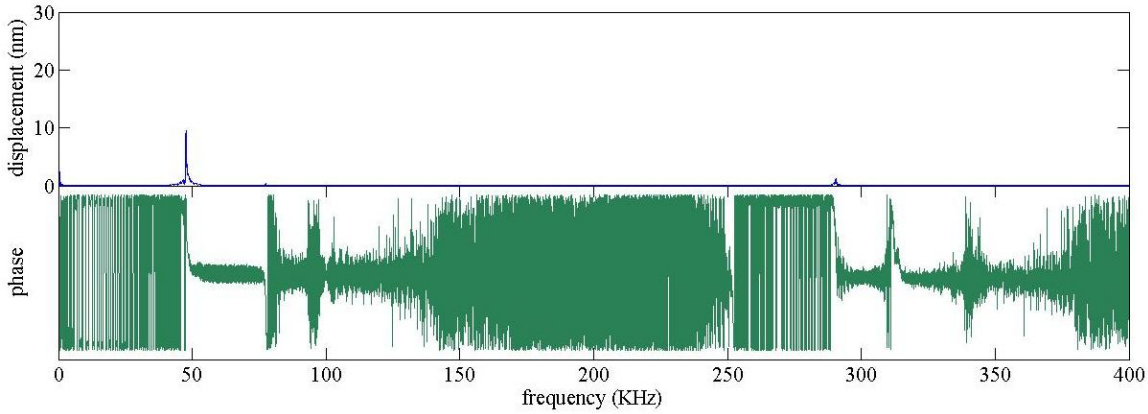


Figure 7.9: Frequency response of beam as measured in laser vibrometer for the beam dimension: length l_b = 250 μm, width w_b = 35 μm having 3 strengthening ridges beneath the beam

for the final mechanical chip design. During the fabrication of these test structures, it was observed that the beam structures with serpentine and folded flexures are more susceptible to the effects of residual stress. In addition to that, during measurements of these structures, the springs are more likely to remain stuck to the substrate once reaching the pull-in voltage, although the beams have the tendency to return to its normal position once the voltage is reduced.

Moreover, since the main requirement of this research is to design and realise a fast switching mechano-optical modulator, high preference is given to the beam-spring structures with relatively high pull-in voltage in the order of 50 to 70 V. With these details obtained from the test structures, the final mechanical beam to be integrated with the optical waveguide is designed and is described in detail in Section 6.5 in Chapter 6.

7.3 Fabrication of Optical Wafer

The outline of the fabrication process of an A-shape TripleX waveguide is shown in Figure 7.10 [5]. The processing is done on silicon substrate containing 8 μm thick thermal oxides, which acts as the lower cladding of waveguide. The fabrication process starts with the deposition of Si_3N_4, which forms the high-index outer core and is followed by the deposition of TEOS oxide, the low-index inner core. Photolithography is then performed followed by the reactive ion etching (RIE) of TEOS SiO_2 and Si_3N_4. In this layer, in addition to the waveguide core design, anti-stiction bumps were also included, which will

prevent the stiction of mechanical element to the waveguide. After removal of photo resist, a second deposition of Si_3N_4 is performed. Finally, an 1100 nm of TEOS and a very thick layer of PECVD (4 μm) oxides are deposited, which forms the upper cladding, see Step 6.

Till this step, the standard process from LioniX BV was used to fabricate the waveguide [5]. Later, the process continues with the post processing of waveguide to integrate the mechanical chip with the waveguide chip. The post processing steps start by performing chemical mechanical polishing (CMP), Step 7 in Figure 7.10, of the top cladding to make it flat. This is followed by the photolithography to open a window of varying size 3x3.001 mm^2, 3x3.002 mm^2 and 3x3.004 mm^2, where, finally the mechanical chip will be clamped to the optical waveguide chip. Next, the top cladding is directionally etched leaving about 200 nm of oxide on top of the core region (see Step 8). The remaining oxide is etched in buffered hydro fluoric acid (BHF) until reaching the waveguide core region.

The complete removal of top cladding on top of the core region is ensured by measuring the surface profile. To avoid scratching the waveguide part while measuring the profile, additional features similar in width as the waveguide core (1 μm) are included in the first mask, whose surfaces are scanned through the profilometer instead of the waveguide core. Also included in this mask are the anti-stiction bumps beside the waveguide. These anti-stiction bumps prevent the beam from damaging the waveguide core during pulled-down state of the mechanical beam and also to prevent from short-circuiting due to gold-gold contact in such pulled-down state. Here, care should be taken to make sure that these bumps are free from gold layer, which otherwise will destroy both the mechanical beam and the optical waveguide when pull-in occurs.

Figure 7.11 shows a SEM image of waveguide with anti-stiction bumps beside it. Next, gold layer needed for the electrodes and electrical connections is deposited using lift off technique. Finally, the optical waveguide chips are separated by dicing. Figure 7.12 shows the micrograph of waveguide with electrodes beside the core for actuation between the mechanical element and the waveguide chip.

7.4 Fabrication of Mechanical Chip to Integrate with the Optical Chip

The fabrication of mechanical chip consisting of suspended beam to be integrated with the optical chip is almost identical to the fabrication of test structures, except for the

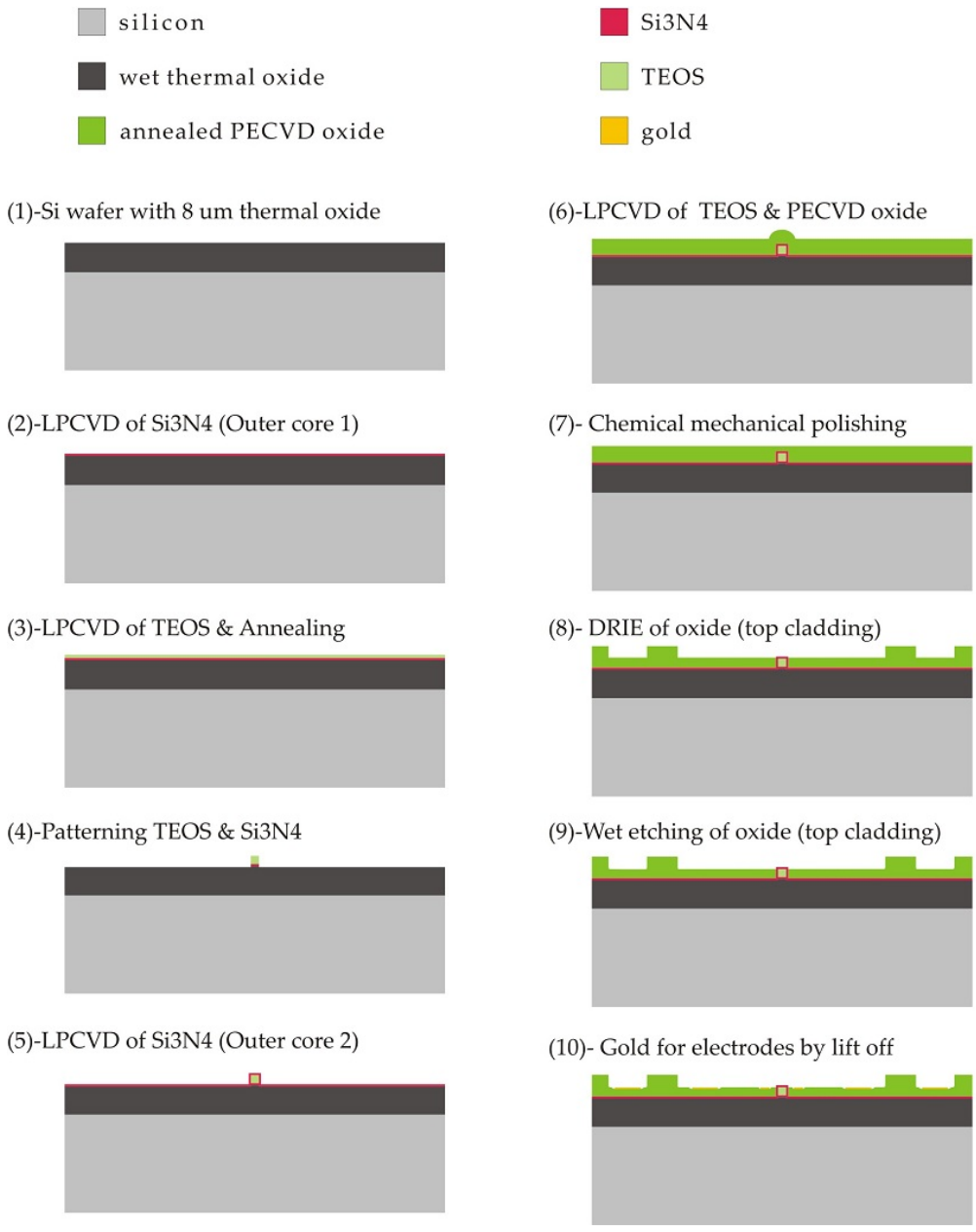


Figure 7.10: Outline of the fabrication process of the waveguide chip [5]

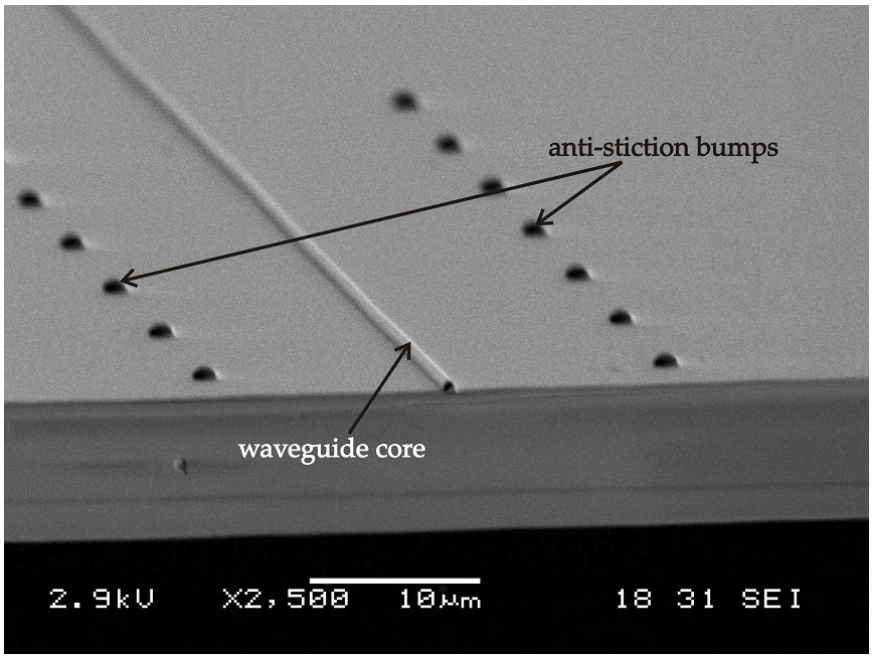
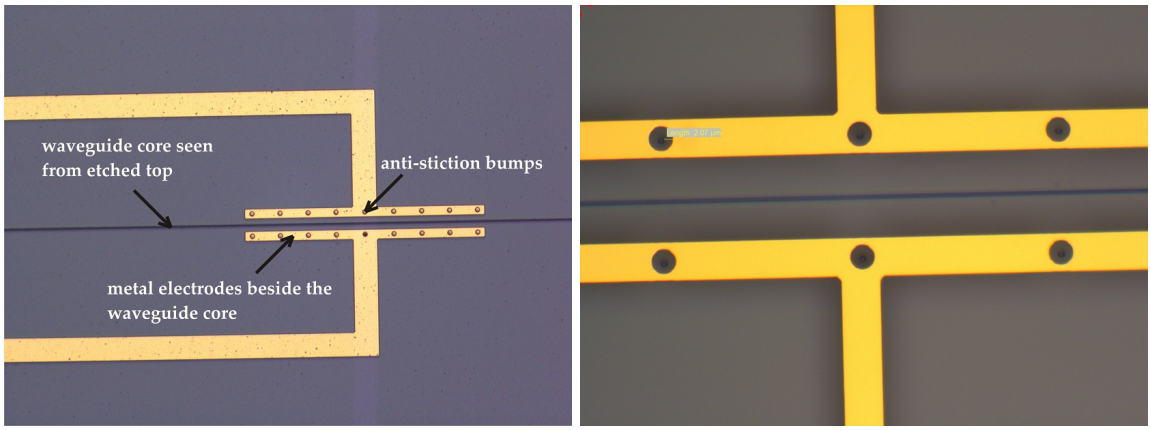


Figure 7.11: SEM image showing the waveguide core with anti-stiction bumps beside it



(a) (b)

Figure 7.12: (a) Microscope image showing the top view of waveguide core with metal electrodes beside it. Also shown are the anti-stiction bumps, which are included to protect the mechanical beam falling on the waveguide core thereby destroying it (b) Close-view of the anti-stiction bumps where the gold is completely removed from them

following steps:

- The process starts with the realization of shallow cavities that define the initial distance between the suspended plate and the waveguide after bonding
- Additional trenches are etched to provide a self-alignment of mechanical chip with the waveguide chip.

The process outline to create the shallow cavities is shown in Figure 7.13. The process starts with the formation of shallow cavities; this is done by local oxidation of silicon followed by removal of the oxide [6]. The fabrication procedure to create the cavities is similar to the process steps followed to create the cavities in <111>-oriented silicon substrate process in Chapter 4 (refer Section 4.2)

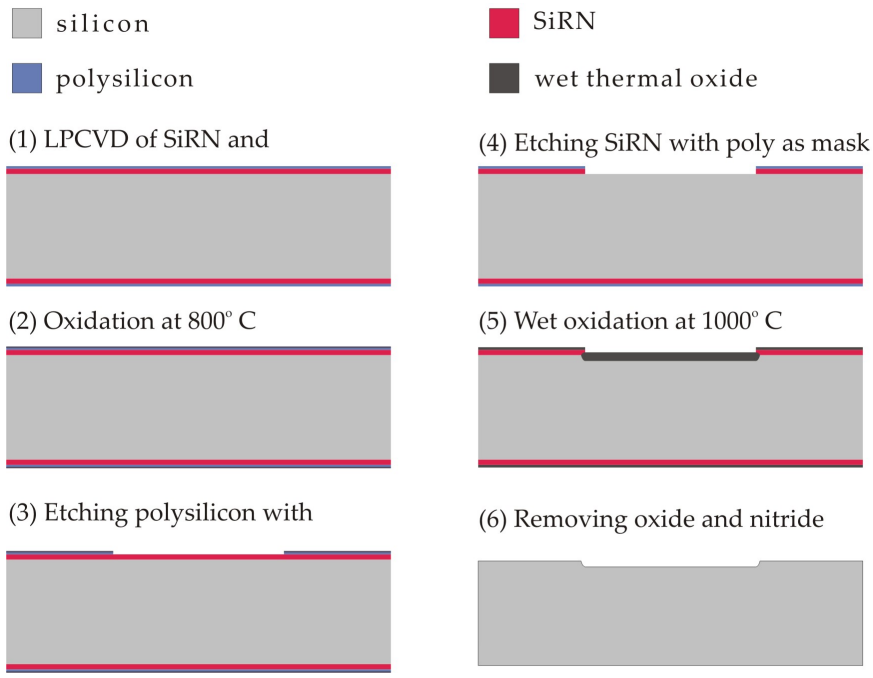


Figure 7.13: Process outline to create shallow cavities in silicon substrate

The process continues from step 7, as shown in Figure 7.14. Though the complete process is kept similar to the test structure fabrication process, there are few additional steps needed to realise the mechanical chip suitable for the integration with the optical waveguide chip. From Step 7 to Step 13, the process followed is similar to as explained in Section 2.4. After etching the Au, Cr and SiRN layers to pattern the mechanical structures, the photoresist is removed in O_2 plasma and in 100% HNO_3. With a new

mask defining the mechanical chip area of 3x3 mm^2, the stack of layers: SiRN, polysilicon, SiO_2 and silicon is etched in Adixen AMS100-SE DRIE etcher, Step 14. The etched sidewall profile of the silicon layer is essential to be vertical, since this should ultimately fit in the cavity created by etching the upper cladding layer in the optical waveguide chip (see Figure 2.10, Steps 8 and 9). The depth of the trench etched in silicon also depends on the depth of cavity created in the optical waveguide chip, which is in the order of ∼5 μm. Again the resist is removed in a combination of O_2 plasma and 100% HNO_3.

After this, with a thick layer of resist, the etched trenches are protected, followed by covering the whole wafer with dicing foil to protect the devices before dicing the chips, refer Step 15. Soon after dicing, the foil was removed keeping the resist at the trenches for its protection during release of the beams in Step 17. The beam with spring structures is released by etching the polysilicon layer using XeF_2. Since the XeF_2 etcher gives the feasibility to do etching in chip level; hence we first dice the chips apart and then release the structures. Moreover, XeF_2 is highly selective to silicon, which requires the corners of the chip (especially the sidewalls of polysilicon and silicon etched in step 8) to be protected in order to avoid any undercut at the edge of the chip, which will introduce any mismatch/misalignment during aligning and clamping. For this purpose, the resist at the trenches were kept until releasing the structures and then removed at the end of the process using O_2 plasma.

In Figure 7.12, top view of one of the released beam with spring structures is shown. Also shown is the undercut in the anchor region due to the etching of polysilicon beneath the SiRN layer during release of structures. The width of the undercut depends on the etching time of polysilicon in XeF_2 etcher. The etching time is optimised so as to etch the polysilicon within the trenches too, so that the ridges underneath the beam are also released completely. The additional trenches shown at the anchor area are included to use as etch stop structures. With this design, the beam, springs and the anchor point are kept in a same level instead of stepped up anchors which is common in fixed-fixed beam structures.

7.4.1 Self-aligned Bonding of Mechanical Chip to Optical Chip

As mentioned earlier, both the optical chips and the mechanical chips are diced prior to bonding, which ensures no broken silicon particles to be trapped in between the bonded

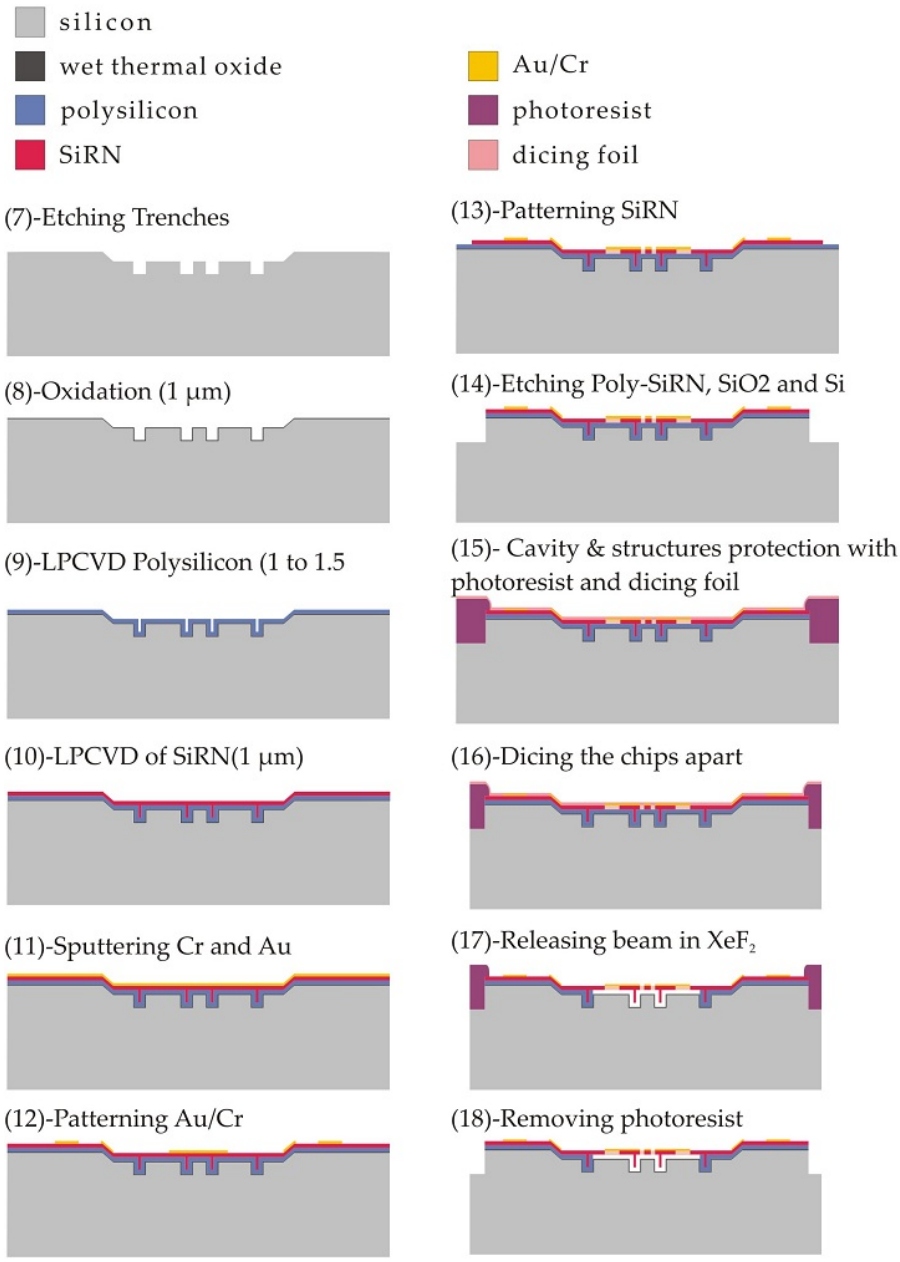


Figure 7.14: Outline of fabrication steps to realise the mechanical chip to be integrated with the optical chip

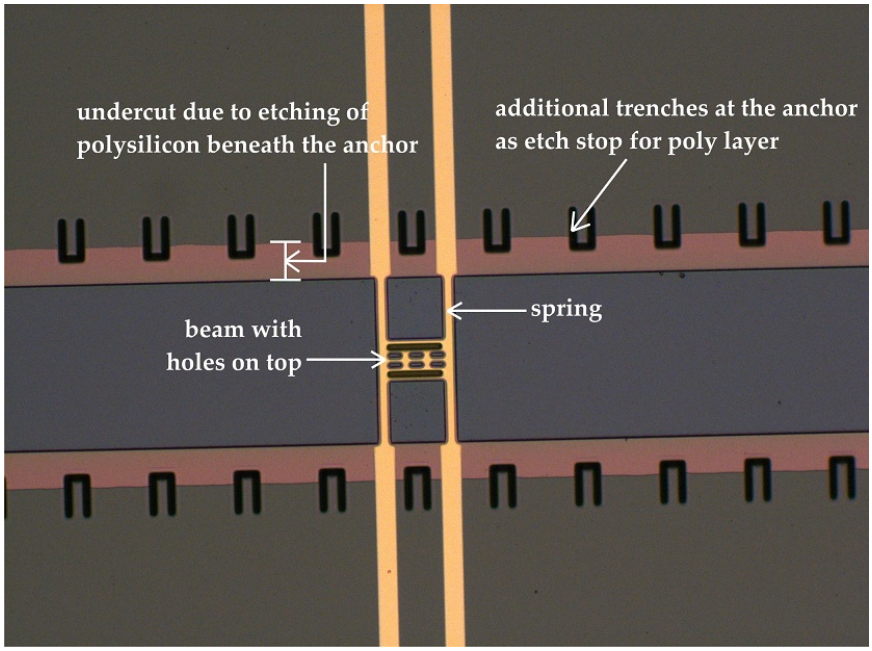


Figure 7.15: Microscopic image showing the top view of one of the released beam with spring structures

area. To align and bond the mechanical chip with the optical chip, few additional steps are required. In the fabrication process of optical waveguide chip described in Section 7.4, after deposition of top cladding layers which is a combination of TEOS oxide and PECVD oxide, the layers need to be flattened using CMP process. The cross section of the waveguide before and after CMP is shown in Figure 7.16 (a) & (b), where the post processing steps needed for self-align bonding are summarised. After CMP is performed, the top cladding layer is patterned with a mask that defines the mechanical chip area, as in Step (c). Finally a gold layer is deposited through lift off process. Prior to this, the oxide layer is etched for about 200 nm. For gold deposition, evaporation is preferred to sputtering, as it is more directional which helps in avoiding residue of metal at the corners.

The total area of the mechanical chip is 3 x 3 mm^2, which will be aligned with the optical chip through the etched cavity that varies in horizontal direction (x) as 3.1-3.4 mm and in vertical direction (y) as 3.004 mm. The increase in the length of about 0.1 to 0.4 mm in x-direction and 0.004 mm in y-direction define the permissible maximum misalignment in the respective directions that are acceptable after bonding.

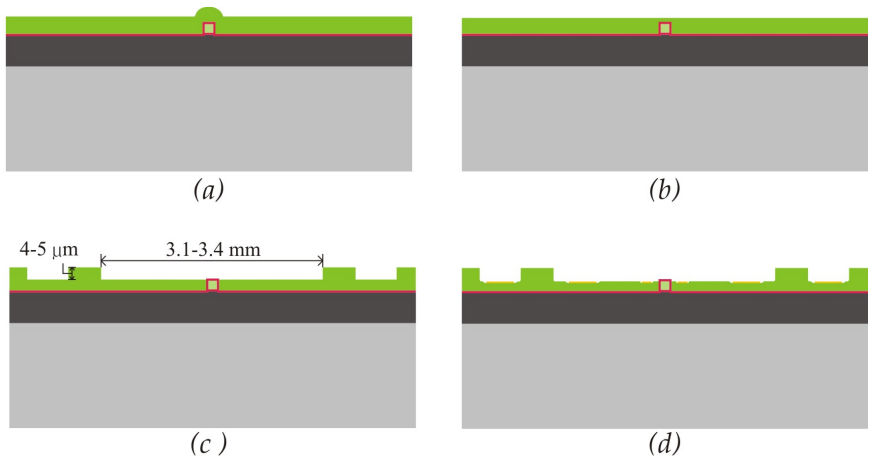


Figure 7.16: Cross sectional view showing the summary of post processing steps that are performed on optical chip for self-align bonding

A drawing showing the top view of the aligned mechanical chip with the optical chip is shown in Figure 7.17. The background shown is the size of the optical chip in which the area measuring 3.1 to 3.4 mm by 3.004 mm is the etched cavity in top cladding, within which the mechanical chip is aligned and clamped to the metal pads. These metal pads also functions as the electrical interconnect for both the optical and mechanical chip. Through these interconnects, the clamping and ultimately the connection between the chips is verified through electrical connectivity.

The procedure of aligning and clamping the mechanical chip with the optical chip is first tested with the test samples of silicon chips measuring 3x3 mm^2 (as mechanical chips) with the etched cavities measuring 3.1 x 3.004 mm^2, 3.2 x 3.004 mm^2 and 3.4 x 3.004 mm^2 in another silicon wafer (as optical chip). After successful fabrication of both the optical and mechanical chips individually, the aligning and clamping of mechanical chips with the optical chips were carried out. Figure 7.18 shows the successfully clamped mechano-optical modulator.

First, the mechanical chip was self-aligned within the cavity of the optical chip, for which the additional markings that were defined in the Au layer on the optical chip were used. When the mechanical chip is aligned and clamped within the cavity in the optical chip, a strip of metal is glued on top of the mechanical chip to hold it from moving out of the cavity due to any external disturbances. The successful aligning and clamping of both the chips are confirmed by measuring the electrical resistance between the electrical interconnects placed across the chip. A close view of the clamped mechano-

optical modulator with wirebonds connecting to the PCB is shown in Figure 7.19.

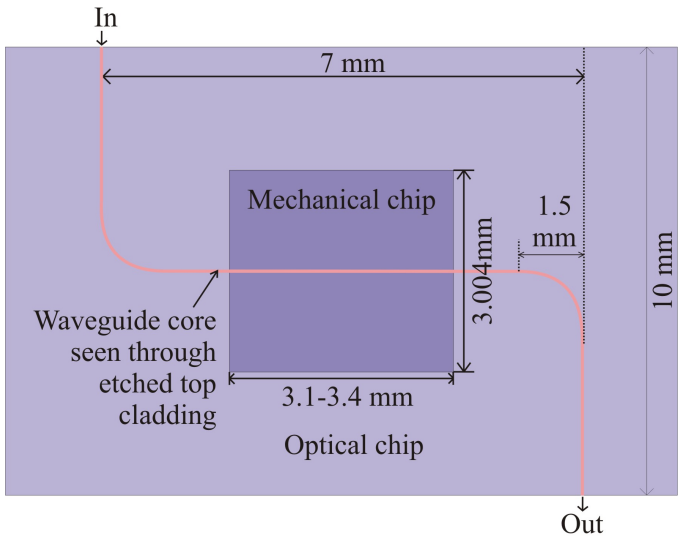


Figure 7.17: Top view showing the aligned mechanical chip with optical chip

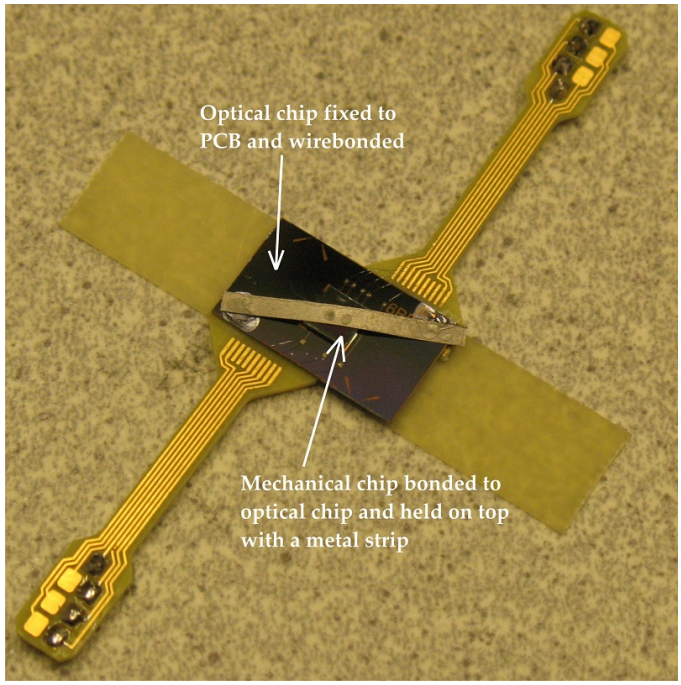


Figure 7.18: Image showing the clamped/bonded mechano-optical modulator and wire bonded to a PCB

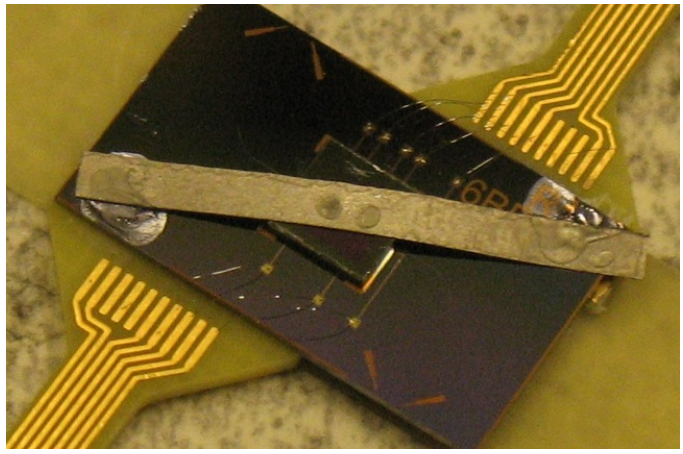


Figure 7.19: Close view image showing the clamped/bonded mechano-optical modulator with wirebonds connecting the optical chip to the PCB and metal glued on mechanical chip to hold it in position

7.5 Conclusion

In this chapter fabrication of mechanical and optical chip are discussed in detail. The fabrication methodology of mechanical chip shown here is promising in terms of rigidness of the beams with ridges underneath them and reproducibility of the fabrication process for the same. The inclusion of these ridges not only adds mechanical stability but has also shown to prevent the stiction of beam during pull-in instability, which has been experimentally demonstrated. From the results obtained in the test structures fabrication, the optimized value for the beam and spring structures has been chosen for the mechanical chip as the perturbing element in the optical modulator. It was also observed that the solid flexure spring structures are more suitable for the integrated optical modulator than the folded or serpentine flexures which are more susceptible towards the residual stress effects. Another likely consequence that could result in these mechanical structures is the charge trapping within the dielectric layers used: SiO_2 and SiRN. This is tested through Capacitance-Voltage (CV) measurements in Chapter 8, where the experimental results of these devices are discussed in detail.

The TripleX waveguide is fabricated using the fabrication process developed by LioniX BV. Ultimately, few post processing steps are necessary in order to deposit gold for electrodes and connection and also to create the cavity to integrate the mechanical chip with the optical chip. Finally, to integrate the developed optical and mechanical chip as a mechano-optical modulator, a novel way of self-aligning the mechanical chip with the

optical chip is also realised and discussed here. This has shown successful aligning and clamping of mechanical chip with the optical waveguide and experimentally confirmed their bonding by measuring the resistance between their electrical interconnects. The characterisation of both the mechanical and optical devices is described in Chapter 8.

7.6 References

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Chapter 8

Towards a Fast Mechano-optical Modulator: Experimental Results and Discussions

Synopsis

Fabrication of the optical and mechanical devices has been performed based on the procedures described in Chapter 7. The optical waveguide and mechanical device were subjected to a series of tests and measurements as summarised below:

- Measurements to study the surface profile of the optical chip and the mechanical chip were performed, which help to examine the difference in the realised structures from the design.
- Electro-mechanical evaluations of the mechanical structures were performed to assess the resonance frequency, and static and dynamic pull-in performances.
- Electrical measurements were performed to study charge-trapping effect in mechanical devices.
- The optical measurements to analyse the insertion losses of the optical waveguide were also performed.
- After the individual measurements of the optical waveguide and mechanical chip, measurements on integrated mechano-optical device were performed.

The results of the aforementioned tests and measurements are discussed in this Chapter. In addition, modelling of the performance of the integrated device is provided based on the information extracted from the measurement results.

8.1 Fabrication Results

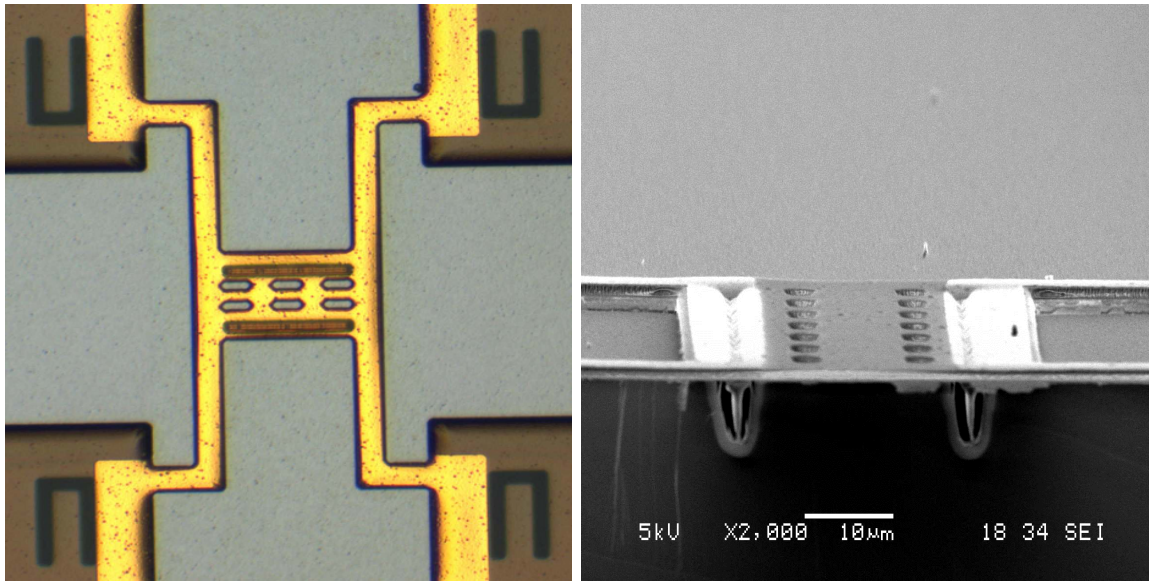
The MEMS structures that resulted from the fabrication schemes described in Chapter 7 are analysed under microscope, White Light Interferometer (WLI) and Dektak surface profilometer. These different analyses are performed on both the mechanical structures and the optical waveguide chips to check their surface profile, before integrating them together through the self-aligned assembly procedure. All measurements described in this section are performed at atmospheric pressure and at ambient temperature.

8.1.1 Surface Profile

Figure 8.1 shows the microscopic image (a top view) and SEM image (cross-sectional view) of the fabricated mechanical structure. Significant roughness can be seen on the top surface of the gold layer on the mechanical beam. For the switching application, the surface roughness on the mechanical beam does not influence the performance as a switch to perturb the optical signal. In fact, it is likely to increase the optical loss introduced into the waveguide when the mechanical beam is pulled down in OFF state due to roughness induced scattering loss. However, in applications such as wavelength tuning using a ring resonator, the surface roughness should be avoided. In an ON/OFF intensity modulator application, more than the roughness, its the waviness on the surface area of the chip and stress on the mechanical beam and gold bond pads on both the chips that influence the function of integrated structure. Both the waviness and stress could increase or decrease the initial separation gap between the mechanical beam and the optical waveguide.

From the images shown in Figure 8.1, it is seen that the mechanical beam remains flat which confirms that it is free from stress induced bending; however the bond-pads, bonding area and overall chip area of both the optical waveguide and the mechanical chip should be tested for any waviness and stress effects. Therefore, before performing hybrid integration, the surfaces of both the optical chip and the mechanical chip are tested under WLI and surface profilometer to assess the waviness and stress induced bending of the beam. Figure 8.2 shows the WLI image of the scanned area on the mechanical chip. The two lines (profile 1 & 2) in the picture show the profiles whose roughness and waviness are calculated from the scanned result. The profiles are chosen close to the electrical bondpads, where the mechanical chip is connected to the optical chip.

The surface roughness and waviness parameters measured for the profiles shown in Figure 8.2 are presented in Figure 8.3. From the scanned result of WLI, it can be observed



(a) (b)

Figure 8.1: Images of mechanical beam (a) Microscopic image showing the top view of the mechanical beam (b) SEM image showing the cross section of the beam, note the flatness of the beam in both the images and the ridges underneath the beam.

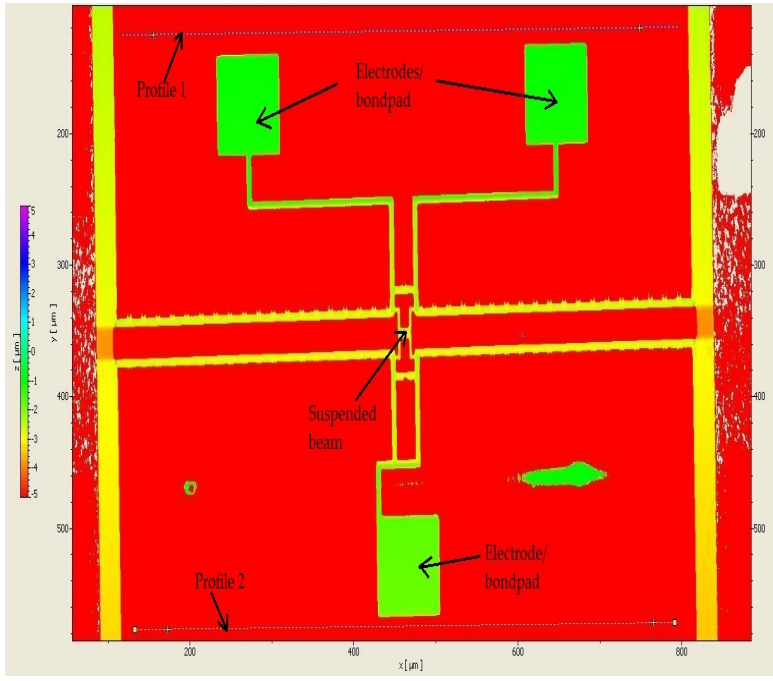


Figure 8.2: WLI image showing the scanned area on the mechanical chip (top line is taken as profile 1 or side 1 and the bottom line as profile 2 or side 2

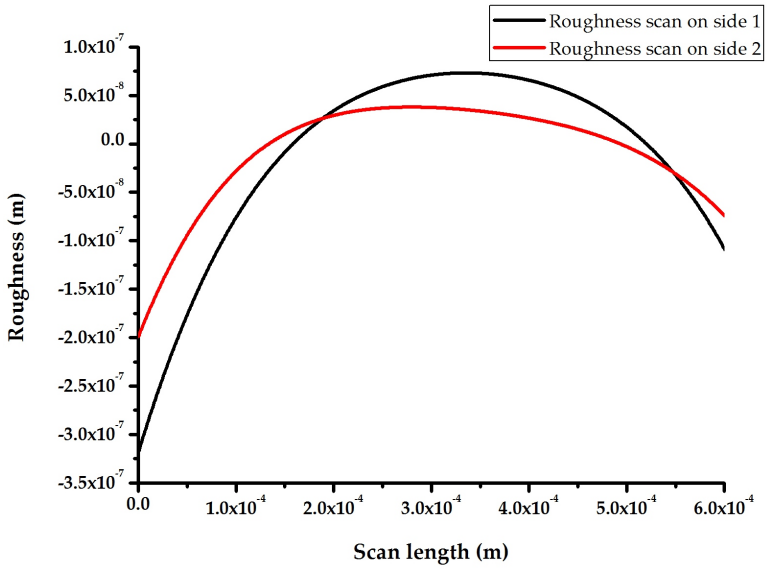


Figure 8.3: Plot showing the roughness of the bonding area and the chip area on the mechanical chip

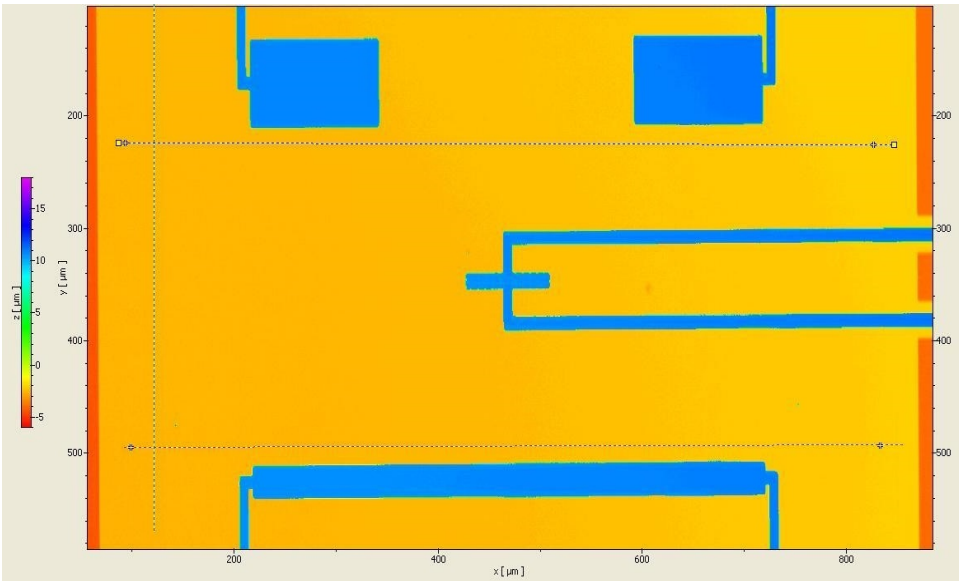


Figure 8.4: WLI image showing the scanned area on the optical chip

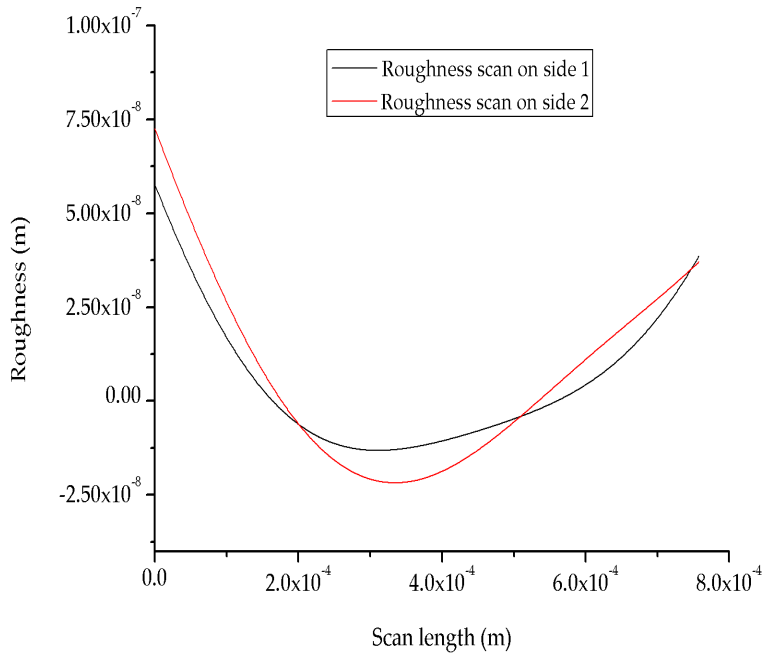


Figure 8.5: Plot showing the roughness of the bonding area including metal bond-pads on the optical chip

that the waviness lies in the order of 350 nm for about 600 μm length beside the bonding area having a peak profile at its centre.

The optical chip is also tested for the presence of any waviness and stress induced bending on the gold electrodes and bond-pads area. Figure 8.4 shows the scanned image from WLI measurement and Figure 8.5 shows the roughness and waviness result of the same. From the profile scan shown in Figure 8.5, it can be observed that it has a valley profile having about 100 nm of waviness for about 800 um of length beside the bonding electrodes. From these results, it is apparent that the waviness over these areas is likely to have an effect on the separation distance between the waveguide and the mechanical beam. Based on Figures 8.2 to 8.5, the separation distance could change by approximately 200 nm.

8.2 Characterisation of Mechanical Structures

The mechanical structures are studied to analyse their electro-mechanical behaviour before integrating them with the optical waveguide chip. The purpose of the electro-

mechanical measurements was to determine the resonance frequency and pull-in voltage of the structures. Capacitance-Voltage (CV) measurements were also carried out to study possible dielectric charging effects in the mechanical beam. In this section, the results of these measurements are discussed. These measurements are performed at atmospheric pressure and at ambient temperature.

8.2.1 Static Pull-in Measurement

The static pull-in measurement is performed by applying a DC voltage between the gold coated SiRN beam and the substrate. The change in the profile of the mechanical beam is measured through the WLI. With an increasing DC voltage, the electrostatic force between the mechanical beam and the substrate increases thereby deflecting the beam towards the substrate. Mechanical structures with different length and spring structures are studied for pull-in measurement. Table 8.1 provides the measured pull-in voltage of different devices along with their dimension and calculated pull-in values. The pull-in voltage is calculated using Equations 6.11 to 6.12 given in Chapter 6. The devices measured had simple beam spring (refer Figure 7.1d) with spring dimensions: length l_{s1} = 100 μm, l_{s2} = 50 μm width w_s = 10 μm and thickness t_s = 1 μm and the calculated spring constant is ~40.01 N/m. The measured spring constant value for different mechanical beams is also given in Table 8.1.

Table 8.1: Measured pull-in voltage of different mechanical devices

Property	Length of beam (μm)	Width μm	Spring Constant measured- (N/m)	Analytical results in MatLab in V	Measured V
	250	35	40.1	17.9	25
Pull-in	125	40	30.866	26.40	24
Voltage	80	40	48.09	46.47	-
(V)	65	35	49.17	56.65	60

The scanned profile of one of the mechanical beam is presented in Figure 8.6. The scanned profile shown in Figure 8.6 is taken at initial condition (V = 0 V) and at pull-in condition (V = 25 V). The fringes seen in the scanned profile at pull-in voltage confirm the bending of beam. The result of the pull-in measurement for a beam having dimensions: L_b = 125 μm, w_b = 40 μm and t = 1μm, is shown in Figure 8.7. The beam pulls down around 24 V, which matches closely with the theoretical calculated value as presented in Figure 6.13 in Chapter 6. Beyond pull-in voltage, the beam remained on the lower fixed electrode

(Si substrate) and when the voltage was slowly decreased, the beam returned back to its original position following a path defined by hysteresis. This shows the interesting aspect of the designed beam having ridges underneath, which reduces the surface area of contact and thereby prevents the beam from sticking to the lower electrode (substrate). This characteristic of the mechanical beam facilitates in performing the bi-directional actuation of the mechanical beam when integrated with the optical waveguide.

8.2.2 Resonance Frequency Measurement

The mechanical resonance frequency of beams with different length and spring structure is measured using Laser Doppler Vibrometer (LDV, Polytec MSA-400) by applying an AC voltage (periodic chirp signal) to the beam. The measured resonance frequency along with higher order modes of different beam are given in Table 8.2, where also shown are the simulated values of natural frequencies. A typical resonance frequency result from LDV for a beam of dimension: Length $L_b = 65$ μm, width $w_b = 35$ μm and thickness $t = 1$ μm is shown in Figure 8.8.

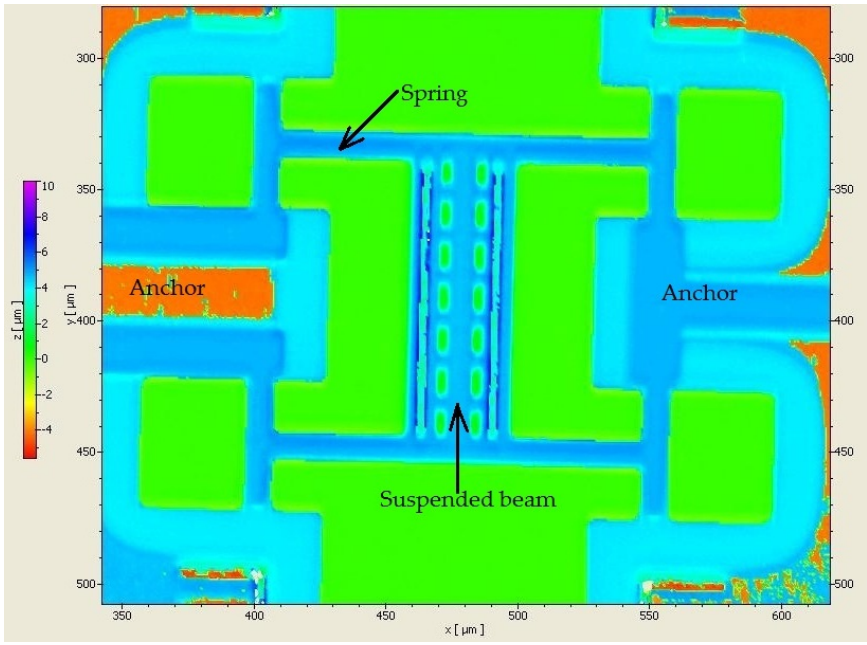
Table 8.2: Measured resonance frequency of different mechanical devices

Natural Frequencies	L_b= W_b=	125μ m 40 μm	L_b= W_b=	80μ m 40 μm	L_b= W_b=	65μ m 35 μm
	FEM results* (MHz)	Measured results (MHz)	FEM results* (MHz)	Measured results (MHz)	FEM results* (MHz)	Measured results (MHz)
Mode 1	0.228	0.198	0.36	0.301	0.421	0.347
Mode 2	0.41	0.397	0.584	0.736	0.698	0.695
Mode 3	0.801	0.596	1.19	1.472	1.403	1.02

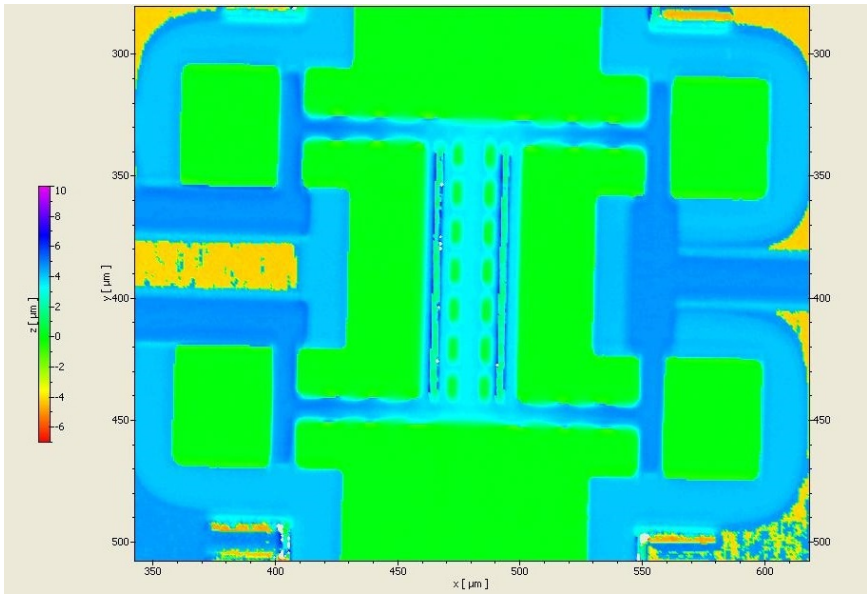
*FEM simulations were performed using Intellisuite software

8.2.3 Dynamic Measurement of the Pull-in Voltage

The dynamic measurement of the pull-in voltage is performed by first applying a small AC voltage to excite the beam and in addition an external DC voltage is applied. With the increasing DC bias voltage, shift in resonance frequency is measured using LDV. The



(a)



(b)

Figure 8.6: WLI scanned profile images (a, top) profile of mechanical beam at V = 0 V & (b, bottom) profile of mechanical beam at V = 25 V

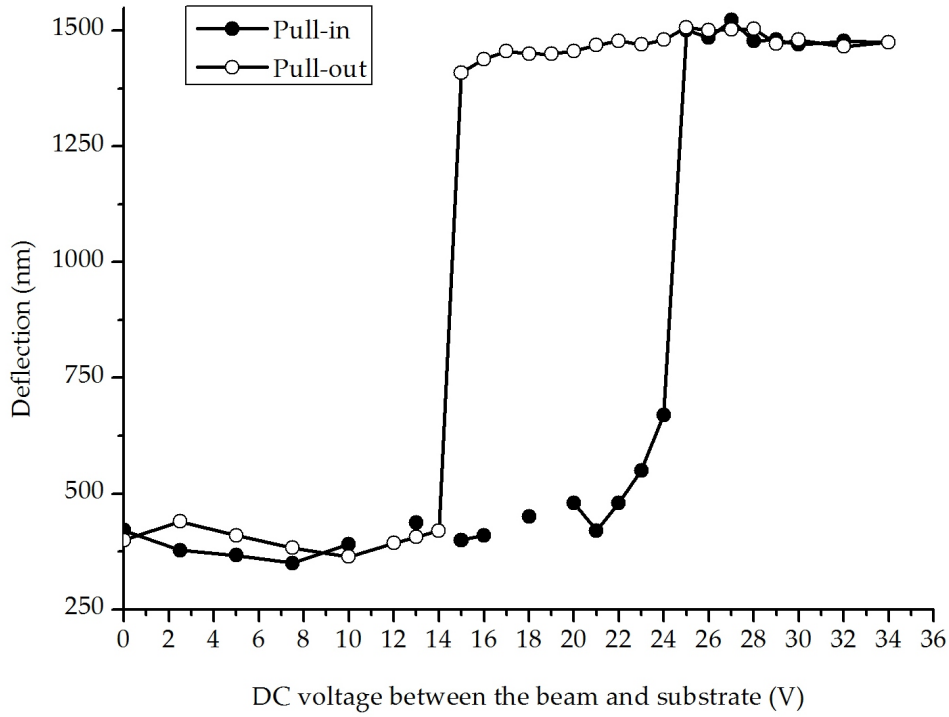


Figure 8.7: Displacement as a function of applied voltage for the mechanical beam. Note the beam pulls down around 24 V.

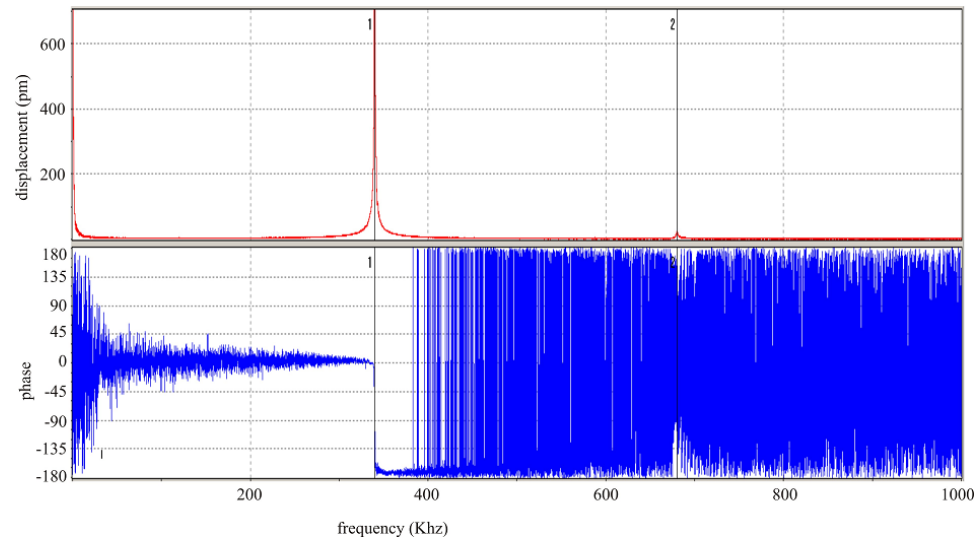


Figure 8.8: Frequency response as measured by LDV for a 65 μm long beam

result of this measurement for a beam of dimension: Length $L_b = 125$ μm, width $w_b = 40$ μm and thickness $t = 1$ μm is shown in Figure 8.9. It is observed that the pull-in voltage measured in this experiment is around 24 V, which is same as observed in the static pull-in measurement.

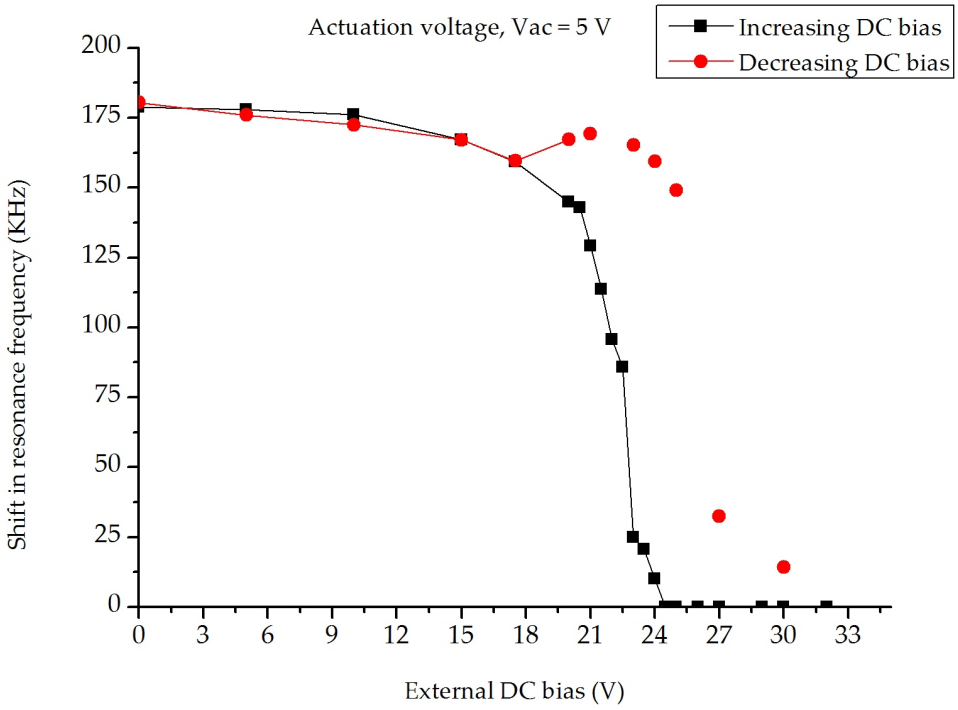


Figure 8.9: Shift in resonance frequency with increasing external DC bias voltage

The resonance frequency shift for a mechanical beam of dimension: Length $L_b = 125$ μm, width $w_b = 40$ μm and thickness $t = 1$ μm at different V_{dc} (0 V, 5 V, 10 V, 15 V, 20 V, 25 V) is shown in Figure 8.9. From this Figure, it is clearly seen that the increase in DC voltage increases the amplitude of vibration, but decreases the resonance frequency, which is due to spring softening effect.

8.2.4 Capacitance-Voltage (CV) measurement

The CV measurements of the mechanical beam are mainly carried out to verify the effect of charge trapping in mechanical structures. Capacitance is measured by applying a bias voltage between the mechanical beam and the highly conductive silicon substrate. The result of this test is shown in Figure 8.11, where the plots of different runs are shown. From these plots, it is observable that the capacitance minimum can shift between

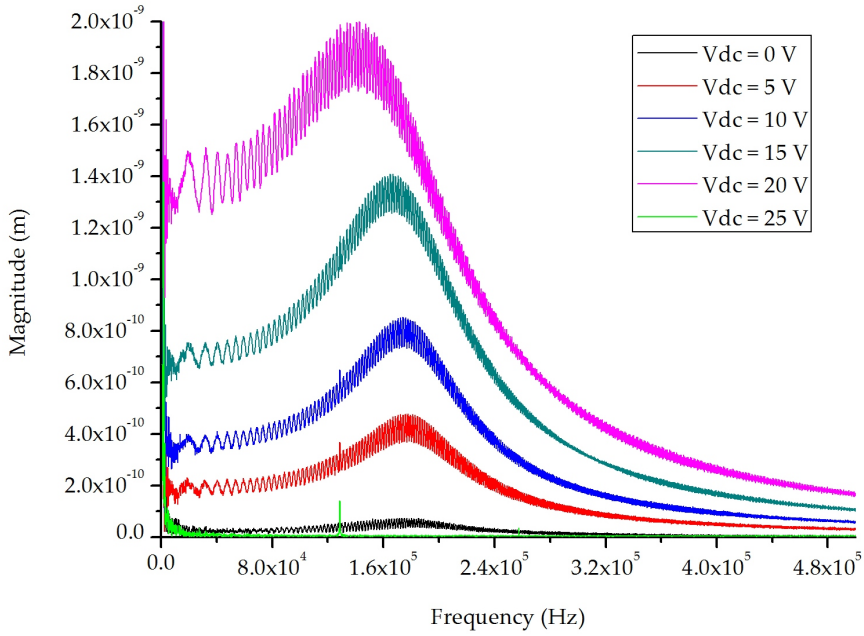


Figure 8.10: Shift in the first mode resonance frequency with increasing DC bias voltage

approximately -5V and +5 V, which confirms that there is a significant amount of trapped charges in these devices and therefore actuation with DC voltages needs to be avoided.

8.3 Characterisation of Optical Waveguide Chip

Figure 8.12 (a) shows the photograph of the set-up used for the optical measurement. The optical chip is placed on a vacuum chuck in order to keep it stable during light coupling and also during measurement. The input and output fibres are fitted in an automatic position controller which facilitate to perform the fine alignment. A Polarization Maintaining Fibre (PMF) is used to launch the light signal into the optical waveguide. The transmitted light from the waveguide is collected through the output fibre into the photo-detector (Agilent 8164B and 8163B). An index matching gel was used at the interface of fibre and waveguide to enhance the coupling. A red laser source (632 nm) is used at the end of both input and output fibres to perform the initial alignment to couple the light into the waveguide. Once initial alignment is done, the red light is replaced with the infra-red light from a tuneable laser source. Figure 8.12 (b) shows the propagation of 632 nm red light through the waveguide.

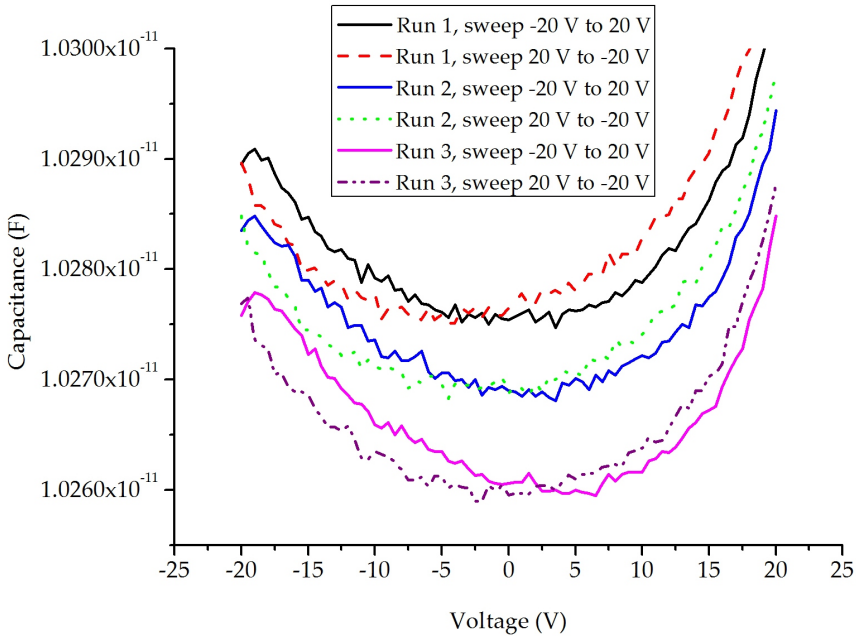
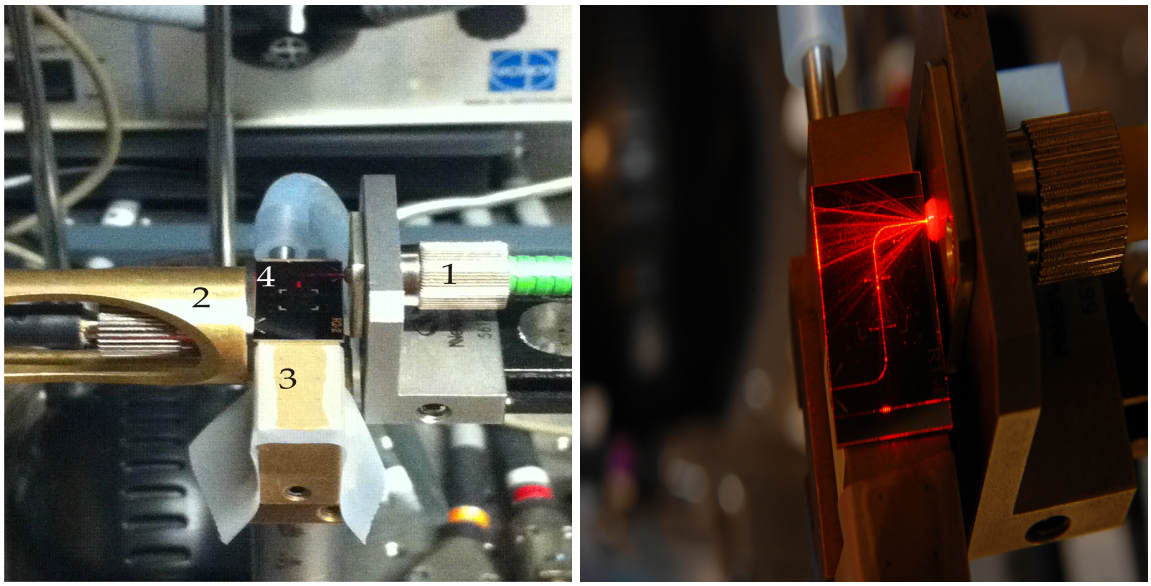


Figure 8.11: CV measurement for a mechanical structure of length 125 µm



(a) (b)

Figure 8.12: Photographs of the set-up used to characterise the optical waveguides (a) 1. Input fibre, 2. Output fibre, 3. Vacuum chuck, 4. Optical Chip & (b) propagation of red light through the optical waveguide

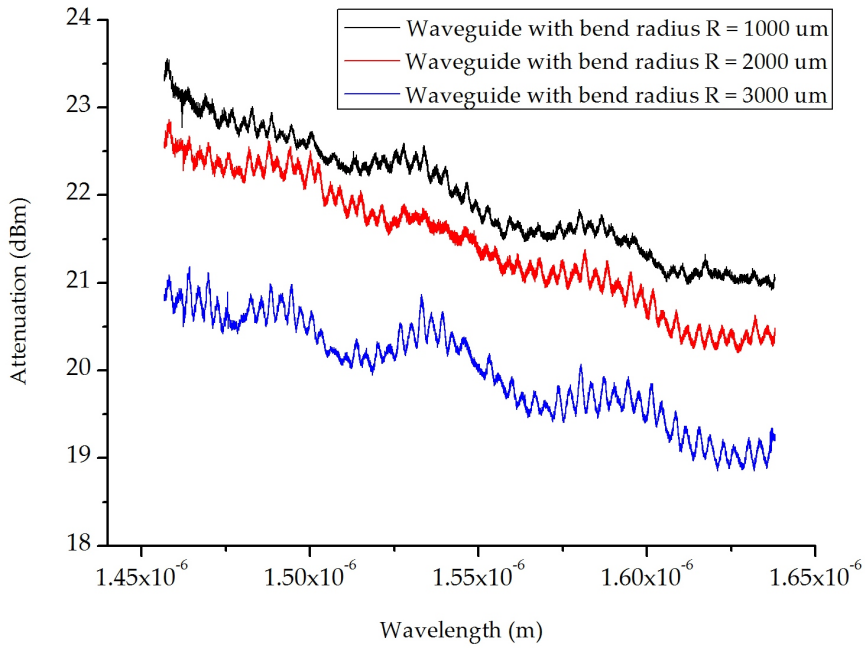


Figure 8.13: Plot showing insertion loss of waveguides with different bend radii

The optical waveguides measured here show insertion loss in the range of 18-25 dB/cm. Three different waveguides having different bend radius in their propagation path are measured. Figure 8.13 shows the measured insertion loss for three optical waveguides having three different bend radiuses. From the insertion loss result shown in Figure 8.13, it is seen that the loss increases with the decreasing bend radius as expected from the analysis presented in Chapter 6, where in Figure 6.10, it is shown that the attenuation decreases with increasing bend radius.

8.4 Characterisation of Integrated Structure

After characterization of mechanical and optical chips individually, they are assembled together through hybrid integration as described in Section 7.3.1, Chapter 7. The assembled device was characterized by both CV measurements and the optical measurements. The CV measurements showed promising results of the working of bi-directional actuation of the mechanical beam, which confirmed the movement of the beam towards the optical waveguide. Subsequently optical measurements were performed to demonstrate the ON/OFF intensity modulator, however without success. The results of both the CV measurements and the optical measurements are discussed in the following sections.

8.4.1 CV Measurement of the Integrated Device

The schematic representation of the set-up used for the CV measurement is shown in Figure 8.14, which includes the Impedance/gain-phase analyzer (Hewlett Packard 4194A), device under test (DUT) and a 300 V range DC power supply. Using the impedance analyzer, a bias voltage with superimposed AC voltage with a frequency of 50 KHz and 0.5 V amplitude is applied between the mechanical beam and the electrodes beside the optical waveguide as shown in Figure 8.14 (b). This resulted in the movement of mechanical beam towards the optical waveguide, which was confirmed through the measured varying capacitance.

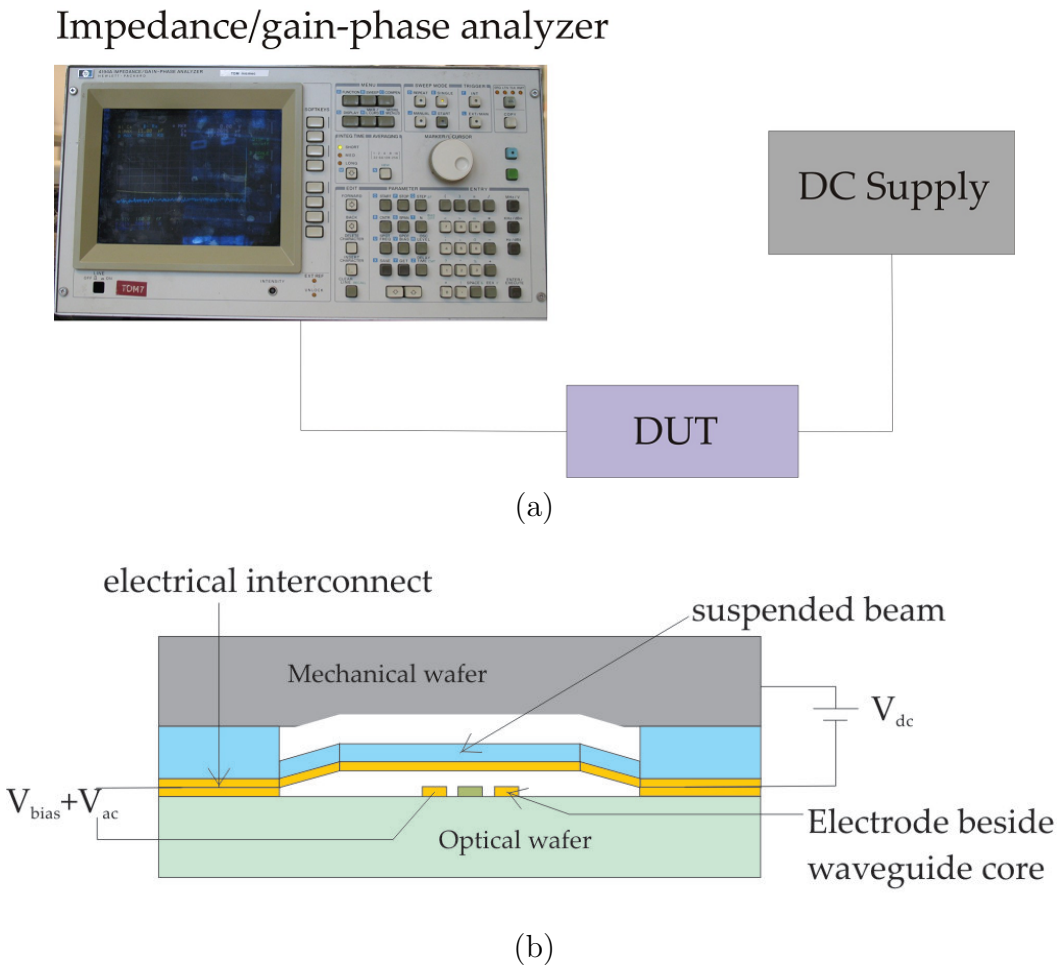


Figure 8.14: (a) Schematic representation of the measurement set-up used for CV measurements (b) connection details of DUT

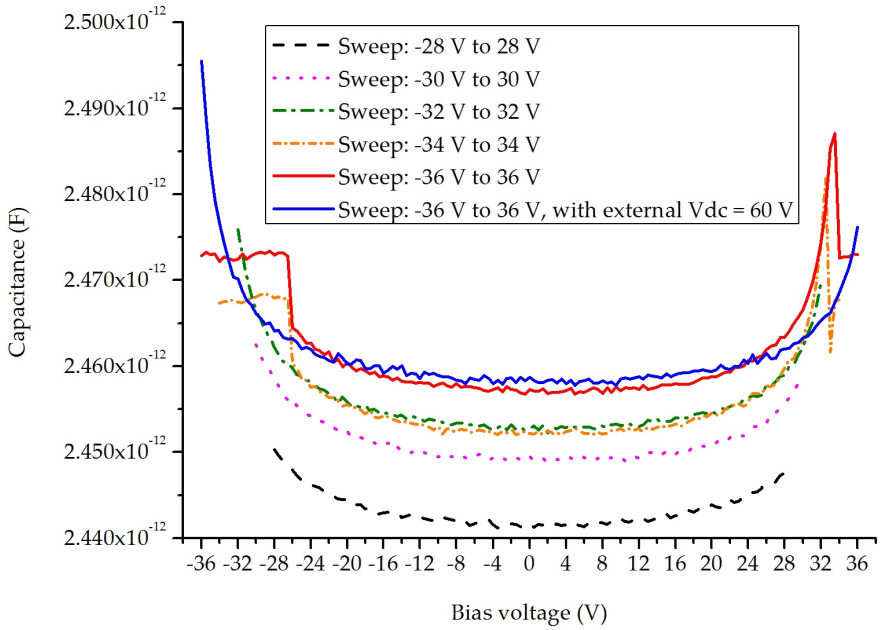


Figure 8.15: CV measurement for a complete assembled device. Voltage is applied between the beam and the electrodes beside the waveguide

Figure 8.15 shows the measured capacitance as a function of applied bias voltage Vbias. At first, the bias voltage was kept well below the pull-in voltage (sweep from -28 V to 28 V) and then it was gradually increased untill pull-in was observed. The voltage sweeps shown here always started at negative voltage and ended at positive voltage. Once the beam is pulled in, using an external supply, a voltage higher than the pull-in (60 V) is applied between the mechanical beam and the highly conductive substrate to which the beam is anchored. This made the beam to be pulled upwards to its original position. The forward movement of mechanical beam towards the waveguide and then towards the substrate (to which the beam is anchored) confirms the bi-directional actuation mechanism. From the results in Figure 8.15, it is seen that the pull-in occurs at lower levels for negative voltages than for positive voltages. Most likely this is due to charging effects as was also observed in the CV measurements presented in Section 8.2.4. The vertical shift between the sweeps, i.e. the change in absolute capacitance value, is most probably due to changing parasitic capacitance values (e.g. due to small changes in temperature).

8.4.2 Optical Measurement of the Integrated Device

Shortly after the CV measurements, the same integrated device was used for the optical measurements. Figure 8.16 shows the schematic of the set-up used for the optical measurements. The measurement was performed at atmospheric pressure and ambient temperature and the DUT was placed on a vibration free table to keep it stable throughout the measurement.

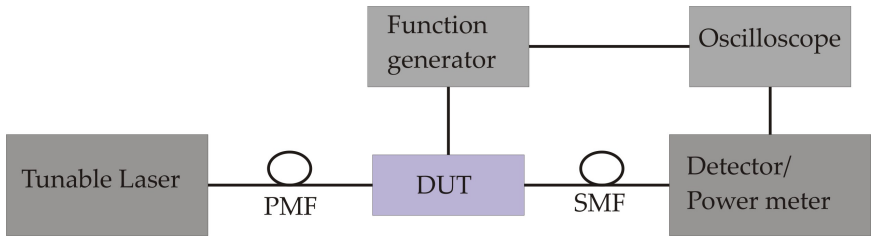


Figure 8.16: Schematic representation of the experimental set-up of optical measurement

With the tuneable laser source, light is launched into the waveguide using a PMF fibre. The transmitted power is collected through a single mode fibre (SMF) into the optical detector (Agilent 8164B and 8163B). The mechanical beam is actuated by applying an AC signal using the function generator. Using the power meter, the optical power is also read. In this experiment, both the transmission and the optical power were measured before and after actuating the mechanical beam. Both the results show that the optical power propagating through the waveguide was undisturbed by the approaching mechanical beam. Further measurements were carried out by actuating the mechanical beam using the impedance/gain-phase analyser which was also used for the CV measurements. This allowed observing both the change in capacitance and the optical power output to the power meter. The CV measurement confirmed the pull-in of the mechanical beam towards the waveguide; however, the optical power output remained the same before and after the beam was pulled in. With this observation, it could be assumed that the gold coated mechanical beam is not disturbing the optical power propagating through the waveguide.

To investigate further, a similar optical waveguide chip was used for the optical power transmission measurement by perturbing the optical signal using an AFM cantilever tip made of different materials such as glass and silicon nitride. This is performed to ensure whether the glass or Si_3N_4 AFM tip could introduce scattering loss in the optical signal. A cantilever having tip dimension of 1μ m was positioned above the protruding core of the waveguide. Once positioned, the cantilever was moved towards the waveguide and

made to touch the core of the waveguide. The AFM tip was also moved laterally over the waveguide core to see any effect. This experiment showed no disturbance in the optical power propagating through the waveguide.

As a further investigation, another experiment was performed using water as a perturbing element to introduce absorption in the waveguide. Before performing this measurement, the power metre was switched ON so that it could keep reading the transmitted power through the waveguide throughout the experiment. Once it is ON, through a syringe a water droplet was placed on the etched top cladding cavity and after some seconds, the water droplet was taken out of the cavity through the syringe. This had introduced an absorption loss in the optical path, which was confirmed through the measurement of the power metre and the insertion loss measurement. The optical power output of the measurement with the water droplet is shown in Figure 8.17. Figure 8.18 shows the insertion loss as a function of wavelength measured before and after placing the water droplet on the waveguide core.

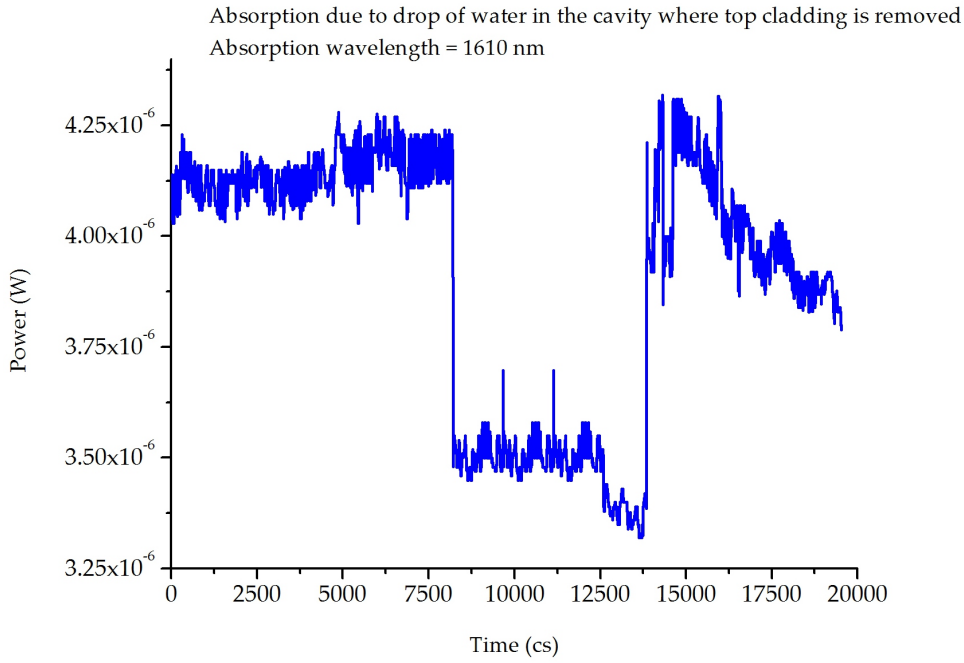


Figure 8.17: Optical power measurement for the experiment with water droplet to perturb the signal propagating through the optical waveguide

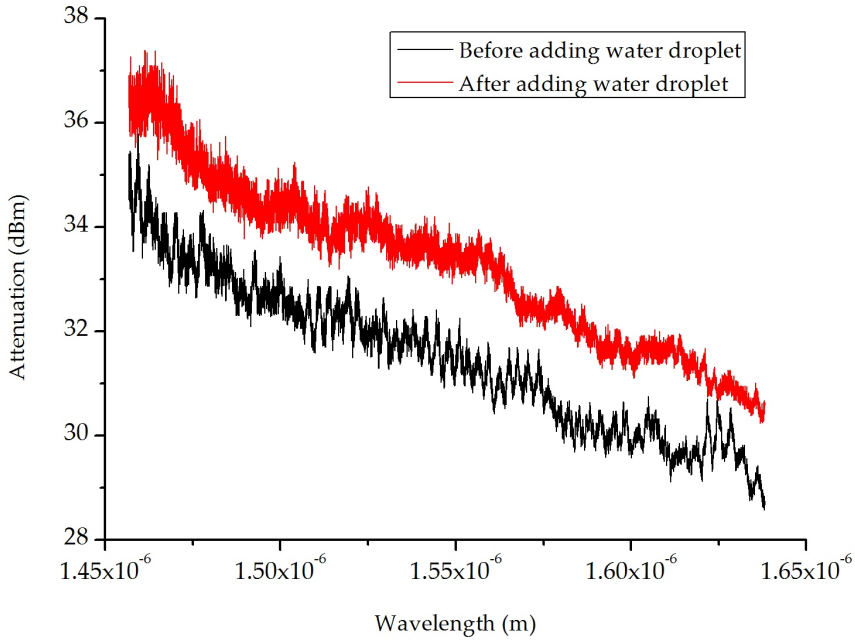


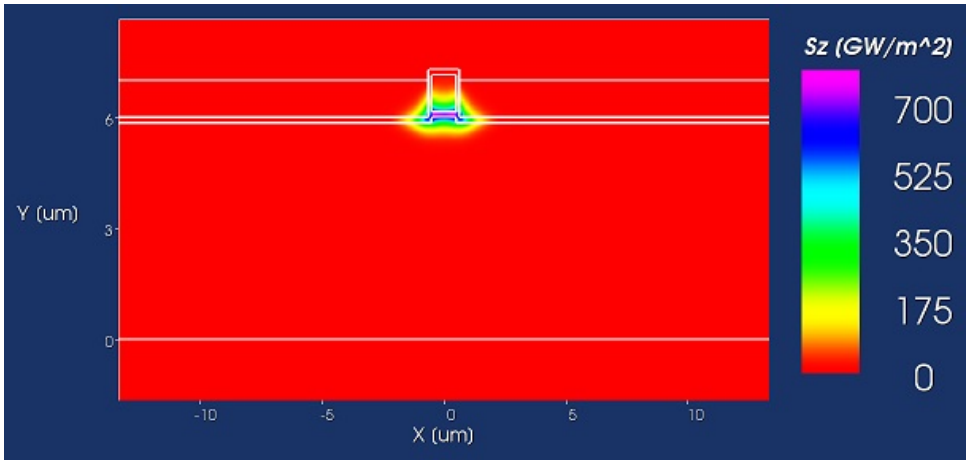
Figure 8.18: Insertion loss measurement before and after perturbing the optical signal using water droplet

8.5 Discussion

The mechanism of introducing loss using gold metal as perturbing element was theoretically demonstrated using Field designer simulations in Chapter 6. However, the results obtained in the optical experiments discussed in previous section do not confirm the functioning of mechano-optical modulator. In the experiments discussed in the previous section, different material combination were used to introduce loss in the path of light propagation in the waveguide; however, the results showed no change in the propagated light except when water is used as perturbing element. This needed further study to understand the behaviour of the optical waveguide design and also the material choice for introducing loss in the optical path to develop mechano-optical modulator.

The dimensions of the fabricated waveguide are given in Table 8.3. In the analyses discussed in Chapter 6, the waveguide design had a top cladding thickness of about 1 μm, whereas in the fabricated waveguide, the top cladding was completely removed. Field designer simulations are performed again for the waveguide dimensions shown in Table 8.3 with different top cladding thicknesses and different Si_3N_4 thicknesses.

Mode field analysis is performed for two different thickness of Si_3N_4 (outer core) 150 nm and 50 nm, and with three top cladding thicknesses viz. 0 nm, 500 nm and 1000



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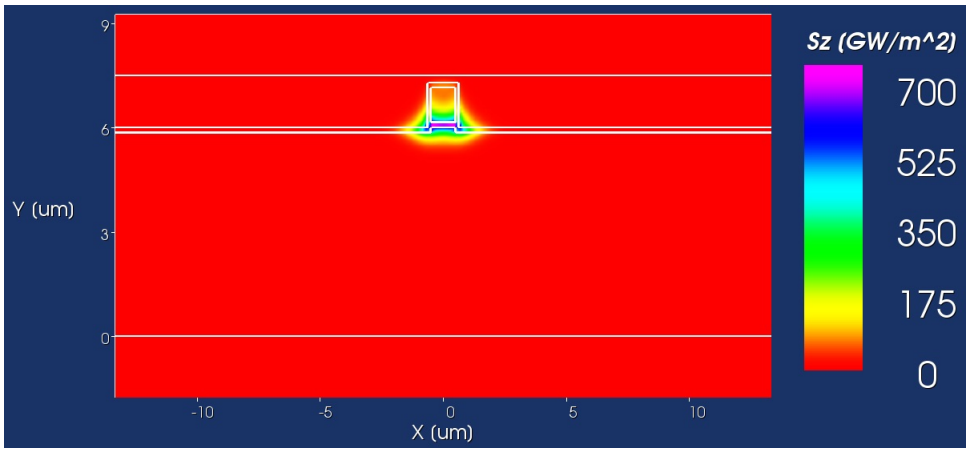

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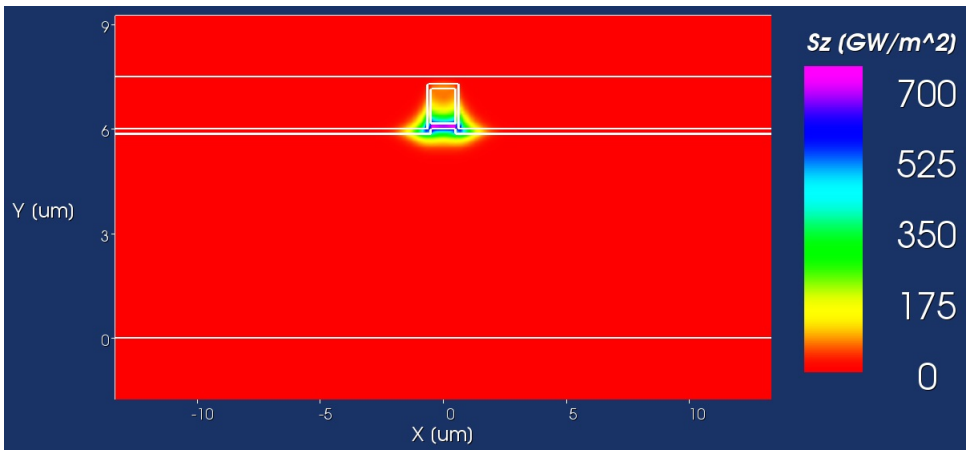
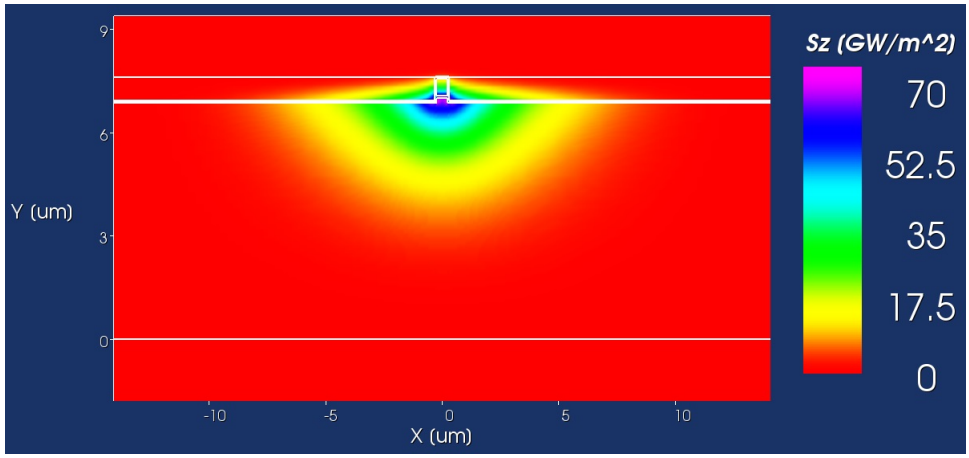


(c)

Figure 8.19: Mode confinement in the waveguide core for Si_3N_4 thickness = 150 nm (a) with top cladding thickness = 0 nm and (b) with top cladding thickness = 500 nm (c) with top cladding thickness = 1000 nm



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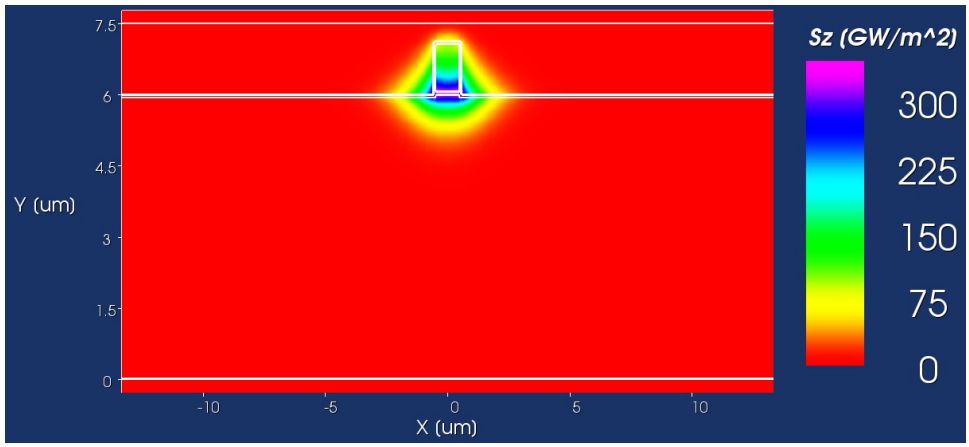

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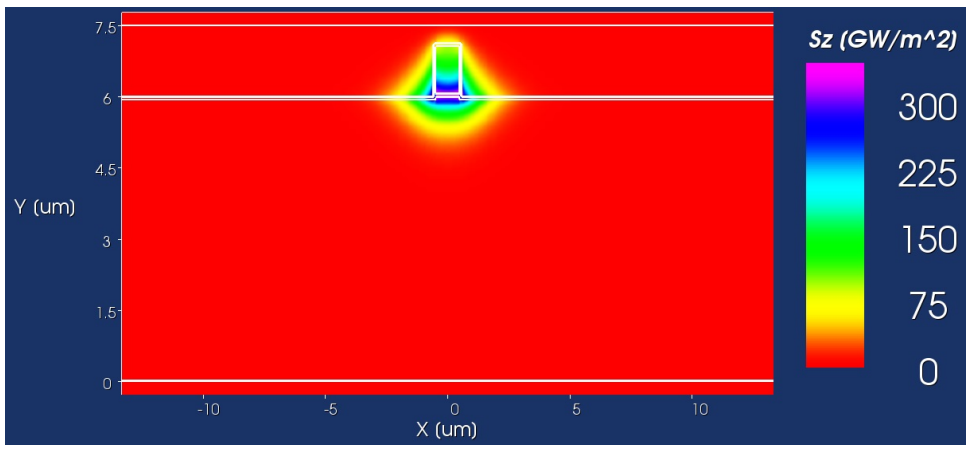

(c)

Figure 8.20: Mode confinement in the waveguide core for Si_3N_4 thickness = 50 nm (a) with top cladding thickness = 0 nm and (b) with top cladding thickness = 500 nm (c) with top cladding thickness = 1000 nm

Table 8.3: Dimensions of fabricated A-shape TripleX optical waveguide

Parameter	Thickness (μm)
Lower cladding oxide	8
Outer core Si_3N_4, first LPCVD	∼0.150
Inner core TEOS	1
Outer core Si_3N_4, second LPCVD	∼0.150
Top cladding	0
Metal Au & Cr	0.110

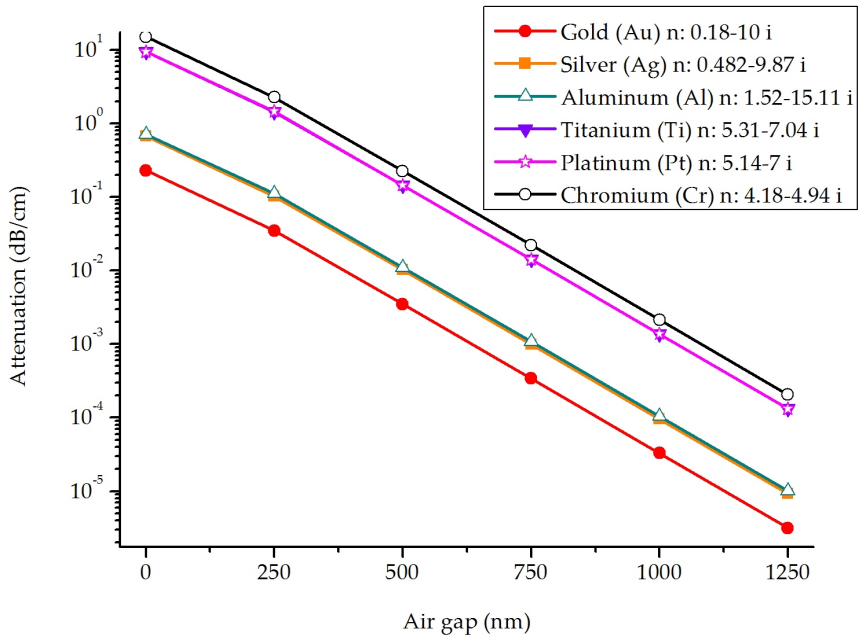

Figure 8.21: Graph showing loss due to different metal type with varying air-gap width

nm. The mode field analyses give the confinement of optical power within the waveguide core. Figure 8.19 shows the mode confinement within the waveguide core for a Si_3N_4 thickness of 150 nm. For 150 nm thick Si_3N_4, it is observed that the optical power is mainly confined within the core for all top cladding thickness. Further, the confinement is especially at the lower part of the core, with almost no power in the evanescent tail above the waveguide. A similar analysis is performed for an Si_3N_4 thickness of 50 nm for the same three different top cladding thickness. Figure 8.20 shows the results

In Figure 8.20, it is observed that the optical power is much less confined within the core. It has spread around the core leaving a significant evanescent tail. Further, the difference in the optical power shown (for different top cladding thickness) is exclusively due to the simulation setting viz. calculation window in the Field designer tool used and not due to the varying top cladding thickness. From these analyses results, it is observed that the thickness of the outer core layer Si_3N_4 has significant effect on the confinement of optical power. It is also observed that a thick Si_3N_4 layer results in a waveguide which is less sensitive to the external disturbances, whereas a thin Si_3N_4 core layer results in a waveguide having a large evanescent tail that is sensitive to external disturbances.

Another study is performed to estimate the amount of loss introduced by different metal layers as perturbing element. This analysis is performed to check whether gold is an optimum metal to introduce absorption loss in the optical path. Mode field analyses were done for various metals as a function of the distance between the metal layer and the optical waveguide. Figure 8.21 shows the calculated loss. From this result, it can be concluded that gold is not the optimal choice and much more absorption loss can be introduced with other metals such as chromium, platinum or titanium.

8.6 Conclusion

Various measurements have shown the following results:

- The surface profile measurements of both the mechanical and optical chips have shown promising results that lead to the successful hybrid integration of the mechano-optical device.

- The electromechanical measurements of the mechanical structures showed that the realised structures closely match with the design. One of the important results here is the pull-in performance of the mechanical structure. In which, the ridges

underneath the beam prevented the stiction of the beam to the lower substrate electrode when pull-in occurred. Both the dynamic and static pull-in performances were performed, which showed the possibility of functioning of mechanical beam as a mechanical switch.

- Electrical measurements are also performed with the mechanical structures to study the effect of charge trapping in them. The CV measurement results showed that the capacitance minimum could shift anywhere between -5 V and 5 V which showed the possibility of trapped charges in these mechanical structures and it is highly essential to avoid actuation with DC voltages.

- The optical measurements were performed to study the insertion loss of the fabricated TripleX waveguides, which showed an insertion loss of 18-25 dB/cm.

- The CV measurement of the complete assembled device was performed to confirm the functioning of bi-directional electrostatic actuation. This measurement also confirmed the movement of the mechanical beam in close vicinity of the waveguide core.

- The optical measurements with the integrated device did not give promising result for the successful demonstration of mechano-optical modulator. However, it leads to further investigation of the waveguide design and the material used for introducing absorption loss in the optical path. Mode field analyses were performed to study the performance of the waveguide and also to find the optimal metal as perturbing element. The results from these analyses show that the waveguide outer core thickness has a significant effect on the mode confinement within the waveguide core and it should be less than the realised waveguide to make it more sensitive to the perturbing element. Furthermore, it can be concluded that gold is not an optimal choice to introduce absorption in the optical path and much better results are expected with chromium, platinum or titanium.

In conclusion, a partly successful demonstration of bi-directional electrostatically actuated mechano-optical modulator is presented in this chapter. From a mechanical and electrical viewpoint the devices performed as expected. However, to materialise the ON-OFF intensity functioning of the mechano-optical modulator, further investigation in the optimal design of the waveguide and the metal layer is essential. The mode field analyses study infers that the realised optical waveguide is rather insensitive to external pertur-

bation and a thinner Si_3N_4 outer core is needed. Further analysis with different metals such as platinum, aluminium and chromium showed that the possibility of introducing loss in the optical path could be much higher with these metals.

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Chapter 9

Conclusions & Recommendation

Synopsis

This chapter gives the summary of the work presented in this thesis and gives some suggestions for further research.

9.1 Introduction

The research presented in this thesis deals with the realisation of micromachined parallel plates separated at sub-micron distance. The parallel plate structures form the basic building block in many applications covering different fields of study viz. Bio-MEMS, RFMEMS, MOEMS etc., In this thesis, micromachined parallel plates are employed to measure the Casimir force and to develop a fast switching mechano-optical modulator. Both subjects involved design study, fabrication and experimental verification of the design and operation principles. In this chapter, concluding remarks are drawn on both topics and some recommendations are suggested for future scope of the research study.

9.2 Casimir Force Measurement

In this work, the focus is given on employing a micromachined parallel plate geometry to measure the Casimir force at sub-micron separation distance. The study involved the design, analysis and fabrication of a parallel plate structure with a separation distance that could be controlled by piezo actuators from about 100nm to 2 μm. A new dynamic measurement methodology has been developed based on using a scanning laser vibrometer (a Polytec MSA-400 system). The scanning laser vibrometer allows monitoring the motion of both plates, one actuated and one suspended by flexures, where the motion of the latter is defined by the forces acting between the plates. The measurement technique and the design of the suspended plate structures were presented in Chapter 3. Further, different measurement schemes were presented that can be applied to measure the Casimir force in terms of plate displacement.

Two fabrication processes were developed, the main difference being the type of substrate that was used, namely <111>-oriented silicon wafers and Silicon-On-Insulator (SOI) wafers. The main purpose of using <111>-oriented wafers was to realize plates with an extremely smooth surface defined by the <111> crystal planes. This was achieved with a combination of DRIE and wet anisotropic etching (using TMAH). Si-Si direct bonding was used to bond the wafers containing the two plates together, so that the final device consists entirely of monocrystalline silicon and is, therefore, relatively insensitive to temperature variations. As expected, the process resulted in ultra smooth surfaces, however the reliability of the process proved to be rather poor due to the DRIE step, as discussed in Section 4.2. The process can be made reliable by using SU-8 100 as an alternate sidewall protecting layer as discussed in Section 4.4.1. It can be concluded that this fabrication

process can indeed result in useful devices, although the SU-8 100 processing still requires some optimisation which was not performed during this work.

The process based on <111>-oriented substrates with the additional process steps could still result in plates with smooth surface which is one of the prime requirements in the Casimir force measurement. However, this process is challenged with many critical steps, besides, the lengthy process also makes it a less viable choice. Further, the SOI process appears more promising in terms of easiness of the process and the strong metal-silicon eutectic bonding of plates that results in sub-micron separation distance, which could make it a more practical choice to realize the parallel plate structures.

The fabrication process based on SOI substrates was mainly developed to result in good fabrication yield and sufficient surface smoothness to do initial experiments. This fabrication process resulted in the successful realization of parallel plate structures with defined separation distance. Despite the fact that the surface roughness of the plates was not quite as smooth as in <111>-oriented silicon process, the yield and reproducibility of the SOI process has been promising. The plates based on the SOI process have a one sided spring, which reduces the complexity of fabrication; however at the expense of reduced mechanical stability. Further, Au-Si eutectic bonding is used in this process to bond the top plate with the bottom plate. This resulted in a strong bond between the plates with the initial distance between the plates remaining in the order of $\sim$1 μm. Although, both fabrication processes resulted in the realization of parallel plate structures, only the devices based on the SOI process were suitable for performing measurements.

Initial characterisation of the fabricated MEMS chips to measure the Casimir force was carried out and the measurement results are discussed in Chapter 5. The devices based on <111>-oriented substrate process resulted in ultra smooth surfaces measuring a roughness in the order of $\sim$3 nm RMS and the waviness in the order of $\sim$20 nm. However, these devices could not be used with the measurement of Casimir force due to an increase in the separation distance between the plates. Devices based on the SOI process resulted in strongly bonded parallel plates separated at $\sim$1 μm distance. With one of these devices, the initial measurements were performed to verify the principle of the Casimir force measurement. The measurement results clearly demonstrated an attractive force between the plates. The bottom plate was actuated and in vacuum environment the top plate moved with opposite phase, that is, decreasing the distance between the plates resulted in an increase of the force between the plates. As expected, at atmospheric pressure, the plates moved in-phase due to the coupling resulting from

the thin air layer between the plates. An unexpected result was that the amplitude of the top plate movement was much larger than predicted without a clear relation to the plate separation. The exact cause of this is still unclear and needs further investigation. Actuation was done at a relatively low frequency, far below any resonance frequencies of the system, so that parasitic coupling through the suspension can be excluded.

In conclusion, the experimental investigation of the Casimir force presented in this thesis looks promising. However, to materialise the measurement of Casimir force with the MEMS chip described in this thesis Chapters 3, 4 and 5, much more measurements are necessary. In the MEMS parallel plate chip assembly set-up used in this thesis study, glue was used to fix the device on the piezoelectric actuator. For future experiments, it is probably better to use a clamping system to mount the parallel plates on the piezoelectric actuator.

9.3 Mechano-Optical Modulator

The second part of this thesis dealt towards the design and realisation of an IONM based mechano-optical modulator to function as an ON/OFF intensity modulator. The major part of this research study dealt with the design and optimisation of a light-weight fast moving mechanical element to be integrated with an optical waveguide to perform as intensity modulator. To this purpose a hybrid integration is used to combine the mechanical part with the optical waveguide. This was successfully carried out using a self-aligned assembly and clamping procedure which was experimentally demonstrated in Chapters 7 and 8 of this thesis. To perform ON/OFF intensity modulation, a lossy (metal) material is introduced in the evanescent part of the optical signal propagating through the waveguide. The concept of this mechanism is theoretically verified using the Field designer mode solver tool developed by PhoeniX BV. Gold as metal is used in the analyses, which showed the feasibility of introducing absorption loss in the optical path. An A-shaped TripleX waveguide developed by LioniX BV has been used as the optical waveguide.

The design of the moving mechanical element has focussed on realising a light weight structure to enable fast movement. An important characteristic of the mechanical structure is the inclusion of ridges underneath the beam. These ridges keep the beam flat and also avoid the stiction of the mechanical beam to the substrate when operated towards pull-in. This functionality is experimentally demonstrated in Chapters 7 and 8. Further,

using bi-directional electrostatic actuation, the suspended mechanical beam is successfully moved towards and away from the waveguide core. This concept is also experimentally demonstrated and the result is shown in Chapter 8.

The TripleX waveguide was fabricated using the fabrication process developed by LioniX BV. This fabrication method required a few post processing steps in order to deposit gold for electrodes and connection and also to create a cavity to integrate the mechanical chip with the optical chip. Finally, to integrate the optical and mechanical chip into a complete mechano-optical modulator, a novel way of self-aligning the mechanical chip with the optical chip was successfully demonstrated. The successful alignment was experimentally confirmed by measuring the resistance through the electrical interconnects.

Using white light interferometer, the surfaces of both the mechanical chip and optical chip were analysed for surface roughness and waviness and the results obtained are promising that lead to the hybrid integration of the chips. The electromechanical measurements of the mechanical structures showed that the realised structures closely match with the design. One of the important results here is the pull-in performance of the mechanical structure, where the ridges underneath the beam prevented the stiction of the beam to the lower substrate electrode when pull-in occurred. Both the dynamic and static pull-in measurements were carried out, which showed the possibility of operating the mechanical beam as a switch. Electrical measurements are also performed with the mechanical structures to study the effects of charge trapping. Capacitance-Voltage (CV) measurements showed that the capacitance minimum could shift anywhere between -5 V and 5 V which showed the possibility of trapped charges in these mechanical structures and therefore actuation with DC voltages should be avoided.

The TripleX waveguides were characterized by measuring the insertion loss, which was in the range of 18-25 dB/cm. CV measurements on the complete assembled device were performed to confirm the functioning of bi-directional electrostatic actuation. This measurement also confirmed the movement of the mechanical beam in close vicinity of the waveguide core. Unfortunately, the movement of the beam did not result in a detectable optical modulation. This led to a further investigation of the waveguide design and the material used for introducing the absorption loss in the optical path. Mode field analyses were performed to study the performance of the waveguide and also to find the optimal metal as perturbing element. The results from these analyses show that the waveguide outer core thickness has a significant effect on the mode confinement within the waveguide core and it should be reduced to make the waveguide more sensitive to the perturbing

element. Furthermore, it can be concluded that gold is not an optimal choice to introduce absorption in the optical path and much better results can be expected with chromium, platinum or titanium.

In conclusion, a partly successful demonstration of a bi-directional electrostatically actuated mechano-optical modulator has been presented in this thesis. From a mechanical and electrical viewpoint the devices performed as expected. However, to materialise the ON-OFF intensity functioning of the mechano-optical modulator, further investigation in the optimal design of the waveguide and the metal layer is essential. The mode field analyses study infers that the realised optical waveguide is rather insensitive to external perturbation and a thinner Si_3N_4 outer core is needed. Further analysis with different metals such as platinum, aluminium and chromium showed that the possibility of introducing loss in the optical path could be much higher with these metals.

List of papers published by the author during the PhD studies

- M. B. Syed Nawazuddin, M. de Boer, J. W. Berenschot, K. C. Ma, M. Elwenspoek and R. J. Wiegerink. 2013. Design, Fabrication and Characterisation of a Suspended Plate Mechano-optical Modulator. *Accepted for presentation in IEEE MEMS 2013*, Taiwan.

- M. B. Syed Nawazuddin, T.S.J Lammerink, J. W. Berenschot, M. de Boer, K. C. Ma, M. C. Elwenspoek and R. J. Wiegerink. 2012. Towards a Casimir Force Measurement between Micromachined Parallel Plate Structures. *Challenges*, 3, pp 261-277.

- M. B. Syed Nawazuddin, T.S.J Lammerink, R. J. Wiegerink, J. W. Berenschot, M. de Boer and M. C. Elwenspoek. 2011. Towards measurement of the Casimir force between parallel plates separated at sub-mircon distance. *Proceedings of the* 16^{th} *International Solid-State Sensors, Actuators and Microsystems Conference, TRANSDUCERS 2011*, 5-9 Jun 2011, Beijing, China. pp. 434-437. IEEE Electron Devices Society. ISBN 978-1-4577-0157-3

- M. B. Syed Nawazuddin, T.S.J Lammerink, R. J. Wiegerink. and M. C. Elwenspoek. 2010. Measurement setup for detecting the Casimir force between parallel plates separated at a sub-micron distance. *Journal of Micromechanics and Microengineering*, 20 (6). 064005. ISSN 0960-1317

- M. B. Syed Nawazuddin, R. J. Wiegerink, T.S.J Lammerink, . and M. C. Elwenspoek. 2009. Parallel plate structures for optical modulation and casimir force measurement. *MME 09 - Proceedings of* 20^{th} *MicroMechanics Europe 2009*, 20-22 September 2009, Toulouse, France. pp. 1-4. Laas-CNRS.

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Appendix A

Process Parameters (Chapter 4)

Table A.1: Process flow based on <111>-oriented substrate for Casimir force parallel plate structures (Chapter 4)

Step	Process		Comment
1	Cleaning Standard	HNO_3 (100%) Selectipur: MERCK HNO_3 (69%) VLSI: MERCK ∘ Beaker 1: fuming HNO_3 (100%), 5min ∘ Beaker 2: fuming HNO_3 (100%), 5min ∘ Quick Dump Rinse <0.1μS ∘ Beaker 3: boiling (95℃) HNO_3 (69%), 10min ∘ Quick Dump Rinse <0.1μS ∘ Spin drying	Standard cleaning of wafer <111>- production, <100>- test wafers
2	LPCVD SiRN - low-deposition rate	Tempress LPCVD new system 2007 program: SiRN01/N2 Tube: G3 ∘ Use 5-8 boat fillers in front and back of the boat to achieve specifications ∘ SiH2Cl2 flow: 155 sccm ∘ NH3 flow: 40 sccm ∘ temperature: 820/850/870℃ ∘ pressure: 150 mTorr ∘ deposition rate: ± 4 nm/min ∘ Nf: ± 2.18 ∘ Stress (range): 200-280 Mpa ∘ Boat position 12: 200 MPa (centre of the boat) ∘Boat position 1: 280 MPa (front of the boat) ∘ Uniformity/wafer: <2% ∘ Uniformity over the boat: (20 wafers): < 8%	Thickness = 100nm check the thickness with dummy wafer Use G4 Time used: 10 mins
3	Ellipsometer Measurement	Plasmos Ellipsometer	Measuring thickness of SiN D1:
4	Cleaning Standard	HNO_3 (100%) Selectipur: MERCK HNO_3 (69%) VLSI: MERCK ∘ Beaker 1: fuming HNO_3 (100%), 5min ∘ Beaker 2: fuming HNO_3 (100%), 5min ∘ Quick Dump Rinse <0.1μS ∘ Beaker 3: boiling (95℃) HNO_3 (69%), 10min ∘ Quick Dump Rinse <0.1μS	

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Table A.1 – *continued from previous page*

Step	Process		Comment
		∘ Spin drying	
5	Micro Balance Measurement	Satotius Micro Balance	Use dummy (without SiN) to measure the polysilicon thickness before and after deposition Mass of D10 (before deposition):
6	LPCVD Poly Si 590℃	Tempress LPCVD Tube: F2 Program: senspoly ∘ SiH4 flow: 50 sccm ∘ temperature: 590℃ ∘ pressure: 250mTorr ∘ deposition rate: xx nm/min ∘ Stress: 30 MPa	Thickness = 50nm (dummy to check the thickness) Time required: 15 mins 30 sec
7	Wet Oxidation at 800℃ of Silicon	Furnace B2 Standby temperature: 800℃ Check water level of bubbler	Oxidizing at standby temperature for 5 mins
8	Lithography - Olin 907-17	Suss Micro Tech Spinner (Delta 20) Hotplate 120 ℃: ∘ Dehydration bake (120℃): 5min HexaMethylDiSilazane (HMDS): ∘ Spin program: 4 (4000rpm, 20sec) Olin 907-17: ∘ Spin program: 4 (4000rpm, 20sec) Hotplate 95 ℃: ∘ Prebake (95℃): 90s EVG 620 Electronic Vision Group 620 Mask Aligner: ∘ Hg-lamp: 12 mW/cm 2 ∘ Exposure Time: 4sec Hotplate 120℃ ∘ After Exposure Bake (120℃): 60sec Developer OPD4262: ∘ Time: 30sec in Beaker 1 ∘ Time: 15-30sec in Beaker 2 ∘ Quick Dump Rinse <0.1μS ∘ Spin drying	Exposure using Mask1: MESA to pattern Polysilicon No hard bake
9	Optical microscopic inspection Lithography	Nikon Microscope	Inspection of resist
10	Etching HF (1%) Native Oxide	HF (1%) VLSI: MERCK 112629.500 ∘ Etch time: >1min ∘ Quick Dump Rinse <0.1μS ∘ Spin drying	Time: 1 min 30 secs (depends on the thickness of oxide)
11	Stripping of Olin PR in Acetone	Acetone VLSI: MERCK 100038 ∘ Spray method, 60-120sec ∘ Spin drying ∘ Visual microscopic inspection	
12	Etching of Silicon by TMAH - standard	TMAH (25%): MERCK 8.14748.1000 A HF (1%) dip must have preceded this etching step ∘ Temp.: 40℃ ∘ Stirrer ∘ Quick Dump Rinse <0.1μS ∘ Spin drying Etch rate (poly-Si) : 60nm/min	Calculated etch rate: 16.67 nm/min
13	Etching HF (50%) LPCVD SiN or Thermal oxide	HF (50%) VLSI: MERCK 100373.2500 ∘ Quick Dump Rinse <0.1μS ∘ Spin drying Etch rate SiRN: 5nm/min	Patterning SiN Etch rate: 4 nm/min

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Table A.1 – *continued from previous page*

Step	Process		Comment
		Etch rate SiO_2: 1 μm/min	
14	Optical microscopic inspection	Nikon Microscope Olympus Microscope Olympus Microscope	Inspecting SiN etching
15	Cleaning Standard	HNO_3 (100%) Selectipur: MERCK HNO_3 (69%) VLSI: MERCK ∘ Beaker 1: fuming HNO_3 (100%), 5min ∘ Beaker 2: fuming HNO_3 (100%), 5min ∘ Quick Dump Rinse <0.1μS ∘ Beaker 3: boiling (95℃) HNO_3 (69%), 10min ∘ Quick Dump Rinse <0.1μS ∘ Spin drying	Cleaning before high temperature process
16	Wet Oxidation at 1000℃ of Silicon	Standby temperature: 800 ℃ Oxidation temp: 1000 ℃	Required oxidation thickness=2500nm Time = 31 hours (previous result) Oxidation rate = 1.34nm/min or 80.67nm/hr
17	Ellipsometer Measurement	Plasmos Ellipsometer	Measure dummy wafer (D9) for oxide thickness. Thickness, D2:
18	Etching HF (50%) user made	HF (50%) VLSI: MERCK 100373.2500 ∘ Temp.: 20℃ ∘ Quick Dump Rinse <0.1μS ∘ Spin drying	Removal of SiO_2, SiN. Inspect the profile to get 1 um mesa structure
19	Cleaning Standard	HNO_3 (100%) Selectipur: MERCK HNO_3 (69%) VLSI: MERCK ∘ Beaker 1: fuming HNO_3 (100%), 5min ∘ Beaker 2: fuming HNO_3 (100%), 5min ∘ Quick Dump Rinse <0.1μS ∘ Beaker 3: boiling (95℃) HNO_3 (69%), 10min ∘ Quick Dump Rinse <0.1μS ∘ Spin drying	
20	LPCVD SiRN - low-deposition rate	Tempress LPCVD new system 2007 ∘ Use 5-8 boat fillers in front and back of the boat to achieve specifications ∘ SiH2Cl2 flow: 77.5 sccm ∘ NH3 flow: 20 sccm ∘ temperature: 820/850/870℃ ∘ pressure: 150 mTorr ∘ deposition rate: ± 4 nm/min ∘ Nf: ± 2.18 ∘ Stress (range): 200-280 Mpa ∘ Boat position 12: 200 MPa (centre of the boat) ∘Boat position 1: 280 MPa (front of the boat) ∘ Uniformity/wafer: <2% ∘ Uniformity over the boat: (20 wafers): < 8%	Thickness=100nm Use Dummy wafer to measure thicknessD3 With G4 = 10 nm/min
21	Ellipsometer Measurement	Plasmos Ellipsometer	Measuring thickness of SiN
22	Cleaning Standard	HNO_3 (100%) Selectipur: MERCK HNO_3 (69%) VLSI: MERCK ∘ Beaker 1: fuming HNO_3 (100%), 5min ∘ Beaker 2: fuming HNO_3 (100%), 5min ∘ Quick Dump Rinse <0.1μS ∘ Beaker 3: boiling (95℃) HNO_3 (69%), 10min ∘ Quick Dump Rinse <0.1μS ∘ Spin drying	Standard cleaning before high temperature process
23	LPCVD TEOS	Tempress LPCVD B4 Tube: B4-TEOS Bubbler: 40.0℃ Temperature: 700℃ pressure: 400mTorr ∘ program: TEOS05 ∘ deposition rate: 10.7 nm/min (25 wafers)	Thickness=1500nm Dummy wafer to measure thickness Deposition rate = 9.81 nm/min Need 1700 nm (Etch rate of TEOS during wafer

Continued on next page

Table A.1 – *continued from previous page*

Step	Process		Comment
		∘ Uniformity/ wafer: 3% ∘ Nf: : 1.44 ∘ stress after deposition: -5 Mpa ∘ stress after two weeks : -20.0 Mpa ∘ Stress after anneal of 700℃: + 5 Mpa	through etching of silicon , since etch rate of TEOS = 56 nm/min)
24	Ellipsometer Measurement	Plasmos Ellipsometer	Measuring thickness of SiO_2
25	Cleaning Standard	HNO_3 (100%) Selectipur: MERCK HNO_3 (69%) VLSI: MERCK ∘ Beaker 1: fuming HNO_3 (100%), 5min ∘ Beaker 2: fuming HNO_3 (100%), 5min ∘ Quick Dump Rinse <0.1μS ∘ Beaker 3: boiling (95℃) HNO_3 (69%), 10min ∘ Quick Dump Rinse <0.1μS ∘ Spin drying	
26	Lithography Dehydration bake SU-8	Hotplate ∘ Dehydration bake (120℃): 10min	Front side Include dummy wafers: bare silicon wafers to be used for plasma etching of Si
27	Lithography Coating SU-8 2005	Sss MicroTec Spinner Delta 20 Microchem NANO SU-8 2005	Thickness=5 μm Spin program:5
	Experimental Results:		
Spin program	**rpm**	**Thickness (μm)**	
1	1000	13.6	
2	1500	8.4	
3	2000	7.4	
4	2500	6	
5	**3000**	**5.2**	
6	3500	4.6	
7	4000	4.1	
28	Lithography - Soft bake SU-8 2005	Hotplate 1 min @ 65 ℃ 2 min @ 95℃	
29	Lithography Alignement & Expo sure SU-8 2005	EVG 620 Electronic Vision Group 620 Mask Aligner ∘ Exposure time 10sec ∘ Hard contact	Mask DRIE Use soft contact
30	Lithography - Post Exposure Bake SU-8 2005	Hotplate ∘ start @ 65 ℃ ∘ ramp to 95 ℃ ∘ cool down to 25℃ ∘ time ca. 90 min	
31	Lithography Development SU-8 2005	TCO Spray Developer Developer: PGMEA (RER600, ARCH Chemicals) ∘ Time: 30 sec with spray-gun, 5 cycles ∘ Time: 5sec rinse with PGMEA bottle ∘ Time: 5sec rinse with IPA ∘ Spin drying	
32	Optical microscopic inspection Lithography	Nikon Microscope	
33	Lithography Hard bake SU-8	Hotplate ∘ 2hr @ 120 ℃	
34	Optical microscopic inspection Lithography	Nikon Microscope	
35	Surface profile measurement	Veeco Dektak 8	Check SU-8 thickness, > 5 microns
36	AdixenSE Plasma etching of SiO_2 and SiRN. Adixen AMS 100 SE Program: CHF3: 100 sccm		New etch time: 7 mins 30 sec

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Table A.1 – *continued from previous page*

Step	Process		Comment
	Ar: 100 sccm ICP: 1200 W CCP: 150 W Electrode: -100 C Etch-rate: 250 nm/min Etch-time: 6 min 30 sec		
37			Depth = 50μm
	Plasma etching of Si C-Cryo-SF6	Adixen AMS 100 SE Program: C.CRYO500 ∘ SF6: 100 sccm ∘ O2: 10 sccm ∘ ICP: 500 W ∘ CCP (pulsed LF): 10 W ∘ On/off: 20/80 (ms) ∘ SH: 200 mm ∘ APC: 100% ∘ He: 10 mbar ∘ Electrode: -100℃ ∘ Etch-rate: ± 2 μm/min Etch-time: 15 min	Dummy wafer first Including inspection (with Adixen)
38	Cleaning "Piranha" (H2SO4/H2O2)	H2SO4 (96%) VLSI: MERCK H_2O_2 (31%) VLSI: MERCK Only use the dedicated wafer carriers and rod. H_2SO_4:H_2O_2 (3:1) vol% ∘ Add H_2O_2 slowly to H_2SO_4 - exothermic process ∘ Adjust the hotplate at 85 ℃, the temperature will increase to 130℃ ∘ Cleaning temperature: 130℃ ∘ Cleaning time 10-15min ∘ Quick Dump Rinse <0.1μS ∘ Spin drying	Removal of SU-8
39			Repeat steps from 25 to 38 for the other side of wafer
40	Etching of SiN (Hot H_3PO_4)	H_3PO_4 85% Merck VLSI 1.00568.2500 Apply always first a Standard Wafer Clean and a 1% HF dip to remove native oxide. ∘ Temp.: 180℃ ∘ Quick Dump Rinse <0.1μS ∘ Spin drying Etch rate SiRN: 3.5 nm/min High selective for SiO_2 layers Only SiO_2, Silicon, Polysilicon, SiRN, SiON, SiON are allowed.	Isotropic pull back of SiN To be etched for a thickness of 50 nm.
Temp (℃)	etch rate SixNy [nm/min]	etch rate (SiO_2) [nm/min]	
180 160 140	4.1 1.4 0.5	0.48 0.16 0.05	
41	Cleaning Standard	HNO_3 (100%) Selectipur: MERCK HNO_3 (69%) VLSI: MERCK ∘ Beaker 1: fuming HNO_3 (100%), 5min ∘ Beaker 2: fuming HNO_3 (100%), 5min ∘ Quick Dump Rinse <0.1μS ∘ Beaker 3: boiling (95℃) HNO_3 (69%), 10min ∘ Quick Dump Rinse <0.1μS ∘ Spin drying	Standard cleaning before high temperature process
42	Wet Oxidation at 900℃ of Silicon	Furnace B2 Standby temperature: 800℃ Check water level of bubbler ∘ Program: WET900 ∘ Temp.: 900℃ ∘ Gas: H2O + N2 (Bubbler)	Thickness=50nm

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Table A.1 – *continued from previous page*

Step	**Process**		**Comment**
43	LPCVD TEOS	Tempress LPCVD B4 Tube: B4-TEOS Bubbler: 40.0℃ Temperature: 700℃ pressure: 400mTorr ∘ program: TEOS05 ∘ deposition rate: 10.7 nm/min (25 wafers) ∘ Uniformity/ wafer: 3% ∘ Nf: : 1.44 ∘ stress after deposition: -5 Mpa ∘ stress after two weeks : -20.0 Mpa ∘ Stress after anneal of 700℃: + 5 Mpa	Thickness=250nm
44	Ellipsometer Measurement	Plasmos Ellipsometer	Measuring thickness of SiO_2, Should be about 1750nm
45	Cleaning Standard	HNO_3 (100%) Selectipur: MERCK HNO_3 (69%) VLSI: MERCK ∘ Beaker 1: fuming HNO_3 (100%), 5min ∘ Beaker 2: fuming HNO_3 (100%), 5min ∘ Quick Dump Rinse <0.1μS ∘ Beaker 3: boiling (95℃) HNO_3 (69%), 10min ∘ Quick Dump Rinse <0.1μS ∘ Spin drying	Standard cleaning before SU-8 100 lithography
46	Lithography Dehydration bake SU-8	Hotplate ∘ Dehydration bake (120℃): 10min	
47	Lithography Coating SU-8 100	Suss MicroTec Spinner Delta 20	Spin speed used
Spin program	**rpm**	**Thickness [μm]±8%**	500 rpm for 30 sec
8	1000	380	2500 rpm for 30 sec
9	1500	230	
10	2000	200	Thickness obtained
11	2500	150	∼130 μm
12	3000	120	
13	3500	100	
14	4000	85	
48	Soft bake Program used: Ramp up to 25℃ with 11℃/min. Stay at 25℃ for 1 hour. Ramp up to 50℃ with 11℃/min stay for 10 mins Ramp up to 65℃ with 11℃/min stay for 30 mins Ramp up to 95℃ with 22℃/min stay for 3 hours and Cool down to 25℃		Leave on hotplate at 20℃ throughout night before exposure.
49	Lithography Alignment & Exposure SU-8 100 (EV620)	EV620 ∘ Electronic Vision Group 620 Mask Aligner ∘ Hg lamp: 12 mW/cm2 ∘ Contact mode: soft contact	Used large gap alignment Time: 65 sec Must use: i-line filter to suppress wavelength below 365 nm, to avoid cracks
	Spin program	**Exposure time [s]**	
	8	120	
	9	75	
	10	67.5	
	11	60	
	12	45	
	13	37.5	
	14	37.5	
50	Post exposure bake:		

Continued on next page

Table A.1 – *continued from previous page*

Step	Process		Comment
	Start at 22℃ Ramp up to 25℃ with 11℃/min stay at 25℃ for 1 hour. Ramp up to 50℃ with 11℃/min stay for 10 mins Ramp up to 65℃ with 11℃/min stay for 10 mins Ramp up to 75℃ with 22℃/min stay for 35 mins and Cool down to 25℃		
51	Lithography Development SU-8	TCO Spray Developer Developer: PGMEA (RER600, ARCH Chemicals) ∘ Cycles: depending on SU-8 thickness ∘ Time: 5sec rinse with PGMEA bottle ∘ Time: 5sec rinse with IPA ∘ Spin drying	Number of cycles: 10 Time/cycle : 1 min
52	Hard bake @ 120℃ for 1 hour		If there are still cracks at sharp edges
53	To remove SU-8 residue Directional O2 plasma etching. Use clean chamber with quartz electrode Power: 50 W Pressure: 0.1 mTorr Temp: 10 degrees O2 flow: 20 sccm		Time: 15-20 mins
54	Plasma etching of SiO_2 (and SiRN)	Adixen AMS 100 SE Program: ∘ CHF3: 100 sccm ∘ Ar: 100 sccm ∘ ICP: 1200 W ∘ CCP: 150 W ∘ Electrode: 20℃ ∘ Etch-rate: 250 nm/min Etch-time: 1 min 30 sec	Bottom removal etching of SiO_2 (thickness=300nm) Dummy wafer first Including inspection (with Etske)
55	Plasma etching of Si A-pulsed-C4F8	Adixen AMS 100 SE Program: ∘ C4F8: 70 sccm ∘ SF6: 400 sccm ∘ ICP: 2500 W ∘ CCP (pulsed LF): 50 W ∘ On/off (ms): 10/90 ∘ SH: 110 mm ∘ APC: 15% ∘ He: 10 mbar ∘ Electrode: 20℃ ∘ Etch-rate: 16 μm/min Etch-time: 30 min (total)	Check recipe with dummy Etch rate: 16.7 μm for opening width: 800 μm Etching has to be done from both sides. Carrier wafer is introduced at the last stage of etching to avoid He leakage.
56	Cleaning "Piranha" (H_2SO_4/H_2O_2)	H2SO4 (96%) VLSI: MERCK H2O2 (31%) VLSI: MERCK Only use the dedicated wafer carriers and rod! H_2SO_4/H_2O_2 (3:1) vol% ∘ Add H_2O_2 slowly to H_2SO_4 exothermic process ∘ Adjust the hotplate at 85 ℃, the temperature will increase to 130℃ ∘ Cleaning temperature: 130℃ ∘ Cleaning time 10-15min ∘ Quick Dump Rinse <0.1μS ∘ Spin drying	SU-8 100 removal. Use one wafer at a time to avoid bumping with other wafers, which later stick together!
57	Repeat steps: 46-56 on back side of wafer.		
58	Etching HF (1%) Native Oxide	HF (1%) VLSI: MERCK 112629.5 ∘ Etch time: >1min ∘ Quick Dump Rinse <0.1μS ∘ Spin drying	Should be done, just before TMAH etching
59	Etching of Silicon by TMAH - standard	TMAH (25%): MERCK 8.14748.1000 A HF (1%) dip must	First test with dummy wafer Etch rate from batch-1: 0.32 μm/min at <111>

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Table A.1 – *continued from previous page*

Step	Process		Comment
		have preceded this etching step Temperature: 70°C Stirrer Rinse in beaker glass with DI-water Rinse in beaker with IPA Dry outside (no spin-drying!)	planes, 1.3 μm/min at <110> planes
		Etch rate (poly-Si) = 60nm/min	
60	Optical microscopic inspection Lithography	Nikon Microscope	
61	Etching HF (50%) user made	HF (50%) VLSI: MERCK 100373.25	Removal of SiO_2, TEOS and SiN.
		Temperature: 20 C Rinse in beaker glass(es) with DI-water Rinse in beaker with IPA Dry (no spin-drying!) Etch-time: 2 min	Time = 22 mins
62	Wet Oxidation at 800°C of Silicon	Furnace B2 Standby temperature: 800°C Check water level of bubbler ◦ Program: standby ◦ Temp.: 800°C ◦ Gas: H2O + N2 (Bubbler)	Thickness: 10 or 20nm Time: 15 mins
63	Optical microscopic inspection - Lithography		

Table A.2: Process flow parameters for carrier wafer (Chapter 4)

Step	Process	Comment
1	Substrate selection Silicon <100> OSP	Supplier: Okmetic Orientation: <100> Diameter: 100 mm Thickness: 525 μm Polished: Single side Type: p
2	Cleaning Standard	HNO_3 (100%) Selectipur: MERCK HNO_3 (69%) VLSI: MERCK ∘ Beaker 1: fuming HNO_3 (100%), 5min ∘ Beaker 2: fuming HNO_3 (100%), 5min ∘ Quick Dump Rinse <0.1μS ∘ Beaker 3: boiling (95℃) HNO_3 (69%), 10min ∘ Quick Dump Rinse <0.1μS ∘ Spin drying
3	Lithography - Olin 907-17	Suss Micro Tech Spinner (Delta 20) Hotplate 120 ℃: ∘ Dehydration bake (120℃): 5min HexaMethylDiSilazane (HMDS): ∘ Spin program: 4 (4000rpm, 20sec) Olin 907-17: ∘ Spin program: 4 (4000rpm, 20sec) Hotplate 95 ℃: ∘ Prebake (95℃): 90s EVG 620 Electronic Vision Group 620 Mask Aligner: ∘ Hg-lamp: 12 mW/cm 2 ∘ Exposure Time: 4sec Hotplate 120℃ ∘ After Exposure Bake (120℃): 60sec Developer OPD4262: ∘ Time: 30sec in Beaker 1 ∘ Time: 15-30sec in Beaker 2 ∘ Quick Dump Rinse <0.1μS ∘ Spin drying
4	Lithography - Post bake 150 ℃	Applications: ∘ Post bake for Cryogenic DRIE to avoid cracking of resist ∘ To fabricate a tapered profile Hotplate 120 ∘ Time: 30min Heraeus Convection Furnace ∘ Temp.: 150 ∘ Time: >15min
5		
6	Stripping of Olin PR by oxygen plasma Tepla 300	Tepla 300 Barrel Etcher (2.45 GHz) Ultra clean system only (no metals except Al) ∘ See list with recipes in CR ∘ O2 flow: 200sccm (50%) ∘ Power: up to 1000W ∘ Pressure: 1 mbar ∘ Time: see recipes on the wall
7	Cleaning Standard	HNO_3 (100%) Selectipur: MERCK HNO_3 (69%) VLSI: MERCK ∘ Beaker 1: fumic HNO_3 (100%), 5min ∘ Beaker 2: fumic HNO_3 (100%), 5min ∘ Quick Dump Rinse <0.1μS ∘ Beaker 3: boiling (95℃) HNO_3 (69%), 10min ∘ Quick Dump Rinse <0.1μS ∘ Spin drying

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Table A.2 – *continued from previous page*

Step	Process		Comment
8	LPCVD SiRN uniform thickness	Tempress LPCVD G3 Program: SiRN01 ∘ SiH2Cl2 flow: 77,5 sccm ∘ NH3 flow: 20 sccm ∘ temperature: 820/850/870℃ ∘ pressure: 150 mTorr ∘ N2 low: 250 sccm ∘ deposition rate: ± 4 nm/min ∘ Nf: ± 2.18 ∘ check validation site for material properties	Thickness = 500nm

Table A.3: Process flow parameters for shadow mask wafer (Chapter 4)

Step	Process		Comment
1	Cleaning Standard	∘ Beaker 1: fuming HNO_3 (100%), 5min ∘ Beaker 2: fuming HNO_3 (100%), 5min ∘ Quick Dump Rinse <0.1μS ∘ Beaker 3: boiling (95℃) HNO_3 (69%), 10min ∘ Quick Dump Rinse <0.1μS ∘ Spin drying	
2	Lithography Olin 907-17	Suss Micro Tech Spinner (Delta 20) Hotplate 120 ℃: ∘ Dehydration bake (120℃): 5min HexaMethylDiSilazane (HMDS): ∘ Spin program: 4 (4000rpm, 20sec) Olin 907-17: ∘ Spin program: 4 (4000rpm, 20sec) Hotplate 95 ℃: ∘ Prebake (95℃): 90s EVG 620 Electronic Vision Group 620 Mask Aligner: ∘ Hg-lamp: 12 mW/cm^2 ∘ Exposure Time: 4sec Hotplate 120℃ ∘ After Exposure Bake (120℃): 60sec Developer OPD4262: ∘ Time: 30sec in Beaker 1 ∘ Time: 15-30sec in Beaker 2 ∘ Quick Dump Rinse <0.1μS ∘ Spin drying	
3	Plasma etching of Si B-ADIX	CR125c/Adixen SE See for profile downloads on the mis homepage	Etch depth observed in run 1 = 80 μm. Requires more than
Parameters	**Etch**	**Deposition**	150 μm depth.
Gas	SF6	C4F8	
Flow sccm	300	150	
Time, sec	7	2	
Priority	2	1	
APC %	25	25	
ICP Watt	1800	1800	

Continued on next page

Table A.3 – *continued from previous page*

Step	Process		Comment
CCP Watt [LF]	80	80	
Pulsed (LF) ms.	10on/90off	10on/90 off	
He (mBar)	10	10	
SH (mm)	200	200	
Electrode temp.(℃)	10	10	
Er Olin907	25-50 nm/min	-	
Er silicon	3-5 μm/min	-	
4	Stripping of Olin PR by oxygen Plasma Tepla 300	Tepla 300 Barrel Etcher (2.45 GHz) Ultra clean system only ∘ See list with recipes in CR ∘ O2 flow: 200sccm (50%) ∘ Power: up to 1000W ∘ Pressure: 1 mbar ∘ Time: see recipes on the wall	
5	Cleaning Standard	NL-CR-WB14 ∘ Beaker 1: fuming HNO_3 (100%), 5min ∘ Beaker 2: fuming HNO_3 (100%), 5min ∘ Quick Dump Rinse <0.1μS ∘ Beaker 3: boiling (95℃) HNO_3 (69%), 10min ∘ Quick Dump Rinse <0.1μS ∘ Spin drying	with 1%HF dip
6	Wet Oxidation at 800℃ of Silicon	Furnace B2 Standby temperature: 800℃ Check water level of bubbler ∘ Program: Oven in standby mode ∘ Temp.: 800℃ ∘ Gas: H_2O + N2 (Bubbler)	Thickness: 10 or 15 nm
7	LPCVD SiRN uniform thickness	Tempress LPCVD G3 Program: ∘ SiH2Cl2 flow: 77,5 sccm ∘ NH3 flow: 20 sccm ∘ temperature: 820/850/870℃ ∘ pressure: 150 mTorr ∘ N2 low: 250 sccm ∘ deposition rate: ± 4 nm/min ∘ Nf: ± 2.18	Thickness: 250 nm Use G4
8	Lithography Olin 907-17	Suss Micro Tech Spinner (Delta 20) Hotplate 120 ℃: ∘ Dehydration bake (120℃): 5min HexaMethylDiSilazane (HMDS): ∘ Spin program: 4 (4000rpm, 20sec) Olin 907-17: ∘ Spin program: 4 (4000rpm, 20sec) Hotplate 95 ℃: ∘ Prebake (95℃): 90s EVG 620 Electronic Vision Group 620 Mask Aligner: ∘ Hg-lamp: 12 mW/cm^2 ∘ Exposure Time: 4sec Hotplate 120℃ ∘ After Exposure Bake (120℃): 60sec Developer OPD4262: ∘ Time: 30sec in Beaker 1 ∘ Time: 15-30sec in Beaker 2 ∘ Quick Dump Rinse <0.1μS ∘ Spin drying	Patterning SiRN Back side
9	Plasma etching SiN (Etske)	Elektrotech PF310/340 Dirty chamber Styros electrode ∘ Electrode temp.: 10℃ ∘ CHF3 flow: 25sccm ∘ O2 flow: 5sccm ∘ pressure: 10mTorr ∘ power: 75W Etchrate SiN : 50nm/min (for VDC=-460V) Etchrate SiN :	Etching Nitride Thickness to be etched = 250 nm. Time used run1: 5 mins

Continued on next page

Table A.3 – *continued from previous page*

Step	Process		Comment
		75 nm/min (for VDC = -580V) Etchrate Olin resist : 95nm/min If DC-Bias < 375V apply chamber clean recipe	
10	Stripping of Olin PR by oxygen plasma Tepla 300	Tepla 300 Barrel Etcher (2.45 GHz) Ultra clean system only (no metals except Al) ∘ See list with recipes in CR ∘ O2 flow: 200sccm (50%) ∘ Power: up to 1000W ∘ Pressure: 1 mbar ∘ Time: 60 mins	Recipe 1 or 6
11	Etching HF (1%) Native Oxide	HF (1%) VLSI: MERCK 112629.500 ∘ Etch time: >1min ∘ Quick Dump Rinse <0.1μS ∘ Spin drying	Etch time: 1 or 2 mins - right before KOH etch
12	Etching of Silicon by KOH - standard	KOH: MERCK 105019.500 KOH:DI = (1:3) 25wt% KOH: 500g KOH pellets in 1500ml DI water ∘ Temp.: 75℃ ∘ Stirrer ∘ Quick Dump Rinse <0.1μS ∘ Spin drying Etch rates: Si <100> = 1μm/min Si <111> = 12.5nm/min SiO_2 (thermal) = 180nm/hr SiRN < 0.6nm/hr	Etch till reaching SiRN structures at front/top
13	Cleaning RCA-2 (HCL/H2O2/H2O)	HCL (36%) Selectipur, BASF H_2O_2 (31%) VLSI, BASF Only use the dedicated wafer carriers and rod $HCL : H_2O_2 : H_2O$ (1:1:5) vol% ∘ add HCL to H_2O ∘ add H_2O2 when mixture at 70℃ ∘ temperature 70-80℃ ∘ cleaning time 10-15min ∘ Quick Dump Rinse <0.1μS ∘ Spin drying	
14	Etching HF (50%) LPCVD SiN or Thermal oxide	HF (50%) VLSI: MERCK 100373.2500 ∘ Quick Dump Rinse <0.1μS ∘ Spin drying Etch rate SiRN = 5nm/min Etch rate SiO_2 = 1 μm/min	Stripping off Nitride layers

Appendix B

Process Parameters (Chapter 4)

Table B.1: Process flow based on SOI wafer for Casimir force parallel plate structures (Chapter 4)

Step	Process		Comment
1	Substrate SOI 25 μm	Supplier: Okmetic Device layer 25 $\pm$0.5 μm resistivity 0.01 - 0,02 ohm.cm Dopant: boron Crystal Orientation: 100 Growth method CZ Oxide layer 1 0.1 μm Handle wafer Growth method CZ dopant boron Crystal orientation 100 Thickness 380 0.5 μm diameter 100 0.5 μm	
2			Field oxide deposition and pattern transfer
3	Surface profile measurement	Veeco Dektak 8	Scan length 80 mm, perpendicular and parallel to the main flat of the wafer. Measure all
4	Measurement of stress of in thin films	Veeco Dektak 8 Applications: o Stress measurements by scanning wafer curvature o Scan length: 80 mm for a 4" wafer o Stylus force: 5 mg o Duration: 60 sec o Profile: hills and Valleys o Use deflection value at 40 mm for stress calculation	SOI wafers. Oxide on the backside of SOI wafer will keep the wafer straight
5	Substrate- Silicon ¡100> OSP	Orientation: ¡100> Diameter: 100mm Thickness: 525μm $\pm$25μm Polished: Single side (OSP) Resistivity: 5-10Ωcm Type: p	Dummy wafers 5 or more
6	Clean HNO_3-1	Beaker 1: HNO_3 (99%) 5min	
7	Clean HN03-2	Beaker 2 : HNO_3 (99%) 5min	
8	Quick Dump Rinse (QDR)	QDR: 2 cycles of steps 1 till 3, 1- fill bath 15 sec 2- spray dump 15 sec 3- spray-fill 40 sec 4- end fill 500 sec Cascade rinsing: continuous flow Rinse till the DI resistivity is $>$ 10 ΩM	

Continued on next page

Table B.1 – *continued from previous page*

Step	Process		Comment
9	Clean HNO_3-3a/b	Beaker 3a/b: HNO_3 (69%), ∘ temp 95℃, ∘ time > 10min	
10	Quick Dump Rinse (QDR)	QDR: 2 cycles of steps 1 till 3, 1- fill bath 15 sec 2- spray dump 15 sec 3- spray-fill 40 sec 4- end fill 500 sec cascade rinsing: continuous flow Rinse till the DI resistivity is > 10 ΩM	In case of using the Semitool for rinsing/drying a single rinsing step (QDR) is required.
11	Substrate drying	Single wafer dryer ∘ speed: 2500 rpm, 60 sec with 30 sec N_2 flow	
12	Dry Oxidation of silicon at 1050℃	Program: N4 - 1050 dry oxidation. Time: 45 min Silicon	Thickness required: 130 - 175 nm for SOI and dummy wafers
Silicon	**(100)**	**(111)**	
Nf	1.467	1.467	
Thick(nm)	76.7	85.0	
3 Sigma	2.97	1.95	
Tmin (nm)	75.2	83.9	
Tmax (nm)	78.6	86.2	
13	Ellipsometer measurement	Plasmos Ellipsometer	Uniformity of oxide layer should be within 5%, measure the oxide layer for all SOI wafers
14	Clean HNO_3-1	Beaker 1: HNO_3 (99%) 5min	
15	Clean HN03-2	Beaker 2 : HNO_3 (99%) 5min	
16	Quick Dump Rinse (QDR)	QDR: 2 cycles of steps 1 till 3, 1- fill bath 15 sec 2- spray dump 15 sec 3- spray-fill 40 sec 4- end fill 500 sec cascade rinsing: continuous flow Rinse till the DI resistivity is > 10 ΩM	
17	Clean HNO_3-3a/b	Beaker 3a/b: HNO_3 (69%), ∘ temp 95℃, ∘ time > 10min	
18	Quick Dump Rinse (QDR)	QDR: 2 cycles of steps 1 till 3, 1- fill bath 15 sec 2- spray dump 15 sec 3- spray-fill 40 sec 4- end fill 500 sec cascade rinsing: continuous flow Rinse till the DI resistivity is > 10 ΩM	In case of using the Semitool for rinsing/drying a single rinsing step (QDR) is required.
19	Substrate drying	Single wafer dryer ∘ speed: 2500 rpm, 60 sec with 30 sec N_2 flow	
20	Micro Balance Measurement	Sartortius Micro Balance	Use dummy wafer to determine polysilicon thickness
21	LPCVD of Poly Silicon @ 590℃	Program: senspoly ∘ SiH4 flow: 50 sccm ∘ temperature: 590℃ ∘ pressure: 250mTorr ∘ deposition rate: 3.4 nm/min ∘ Stress: 30 MPa Maximμm thickness: 2.5 μm	
22	Micro Balance Measurement	Sartortius Micro Balance	Weigh the dummy wafer again with deposited polysilicon and calculate the thickness
23	Inspection by optical microscopic	∘ olympus Microscope ∘ leica Microscope	
24	Wet Oxidation o Silico at 800℃	Standby temperature: 800℃ Check water level of bubbler Check water temp. 85 ℃ Program: Standby ∘ Temp.: 800℃ ∘ Gas: H2O + N_2 (Bubbler)	Continue immediately from previous step for oxidation at 800 degrees for 10 mins.

Continued on next page

Table B.1 – *continued from previous page*

Step	Process		Comment
		∘ N_2 Flow: 2 liter/min ∘ Ramp: 10 ℃/min ∘ Cool down: 7.5 ℃/min	
25	Dehydration bake	Dehydration bake on hotplate ∘ temperature: 120℃ ∘ time: 5min	
26	Priming (liquid)	Primer: HexaMethylDiSilazane (HMDS) use spin coater: ∘ program: 4000 (4000rpm, 30sec)	
27	Coating Olin Oir 907-17	Coating: Primus spinner ∘ olin oir 907-17 ∘ spin Program: 4000 (4000rpm, 30sec) Prebake: hotplate ∘ time 90 sec ∘ temp 95 ℃	
28	Alignment & Exposure Olin OiR 907-17	Electronic Vision Group EV620 Mask Aligner ∘ Hg-lamp: 12 mW/cm 2 ∘ Exposure Time: 4sec	Mask 1 defining oxide layer (provides electrical isolation and Au barrier for eutectic bonding)
29	Development Olin OiR resist	After exposure Bake : hotplate ∘ time 60sec ∘ temp 120℃ Development: Developer: OPD4262 ∘ time: 30sec in Beaker 1 ∘ time: 15-30sec in Beaker 2	
30	Quick Dump Rinse (QDR)	QDR: 2 cycles of steps 1 till 3, 1- fill bath 15 sec 2- spray dump 15 sec 3- spray-fill 40 sec 4- end fill 500 sec cascade rinsing: continuous flow Rinse till the DI resistivity is > 10 ΩM	
31	Substrate drying	Single wafer dryer ∘ speed: 2500 rpm, 60 sec with 30 sec N_2 flow	
32	Post bake Olin OiR resist	Post bake: Hotplate ∘ temperature: 120℃ ∘ time 10min	
33	Inspection by optical microscope	Nikon Microscope ∘ dedicated microscope for lithography inspection	
34	Etching in 1% HF multipurpose	Multipurpose use dedicated Beaker HF 1% ∘ temperature: 20 ℃. ∘ time: depends on application	Etch oxide layer, surface should be hydrophobic after removal of oxide
35	Cleaning acetone & IPA (VLSI)	Removal of organic residue Use ultrasonic bath 2 or 3 ∘ Beaker 1: Acetone VLSI > 10 min , ∘ Beaker 2: IPA VLSI > 10 min ∘ Spin drying	Stripping resist layer. Do not use HNO_3 and/or O2 plasma due to re-oxidation of the silicon surface
36	Substrate drying	Single wafer dryer ∘ speed: 2500 rpm, 60 sec with 30 sec N_2 flow	
37	Etching in TMAH (25wt%)	Use dedicated Beaker : TMAH (25%) standard A HF (1%) dip must have preceded this etching step ∘ temperature: 40℃ ∘ stirrer ∘ Quick Dump Rinse 10.5 MΩ ∘ spin drying	
Material	**Temp**	textbfetchrate	
Poly590	40	60nm/min	
ALN	20	22nm/min	
38	Quick Dump Rinse (QDR)	QDR: 2 cycles of steps 1 till 3, 1- fill bath 15 sec 2- spray dump 15 sec 3- spray-fill 40 sec 4- end fill 500 sec cascade rinsing: continuous flow Rinse till the DI resistivity is > 10 ΩM	
39	Substrate	Single wafer dryer	

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Table B.1 – *continued from previous page*

Step	Process		Comment
	drying	◦ speed: 2500 rpm, 60 sec with 30 sec N_2 flow	
41	Stripping resist in HNO_3 (99%)	◦ Beaker 0: HNO_3 (99%) ◦ time: > 10 min, depends on the application	
42	Quick Dump Rinse (QDR)	QDR: 2 cycles of steps 1 till 3, 1- fill bath 15 sec 2- spray dump 15 sec 3- spray-fill 40 sec 4- end fill 500 sec cascade rinsing: continuous flow Rinse till the DI resistivity is > 10 ΩM	
43	Clean HNO_3-1	◦ Beaker 1: HNO_3 (99%) 5min	
44	Clean HN03-2	◦ Beaker 2 : HNO_3 (99%) 5min	
45	Quick Dump Rinse (QDR)	QDR: 2 cycles of steps 1 till 3, 1- fill bath 15 sec 2- spray dump 15 sec 3- spray-fill 40 sec 4- end fill 500 sec cascade rinsing: continuous flow Rinse till the DI resistivity is > 10 ΩM	
46	Clean HNO_3-3a/b	NL-CR-WB14 Beaker 3a/b: HNO_3 (69%), ◦ temp 95°C, ◦ time > 10min	
47	Quick Dump Rinse (QDR)	QDR: 2 cycles of steps 1 till 3, 1- fill bath 15 sec 2- spray dump 15 sec 3- spray-fill 40 sec 4- end fill 500 sec cascade rinsing: continuous flow Rinse till the DI resistivity is > 10 ΩM	In case of using the Semitool for rinsing/drying a single rinsing step (QDR) is required.
48	Substrate drying	Single wafer dryer ◦ speed: 2500 rpm, 60 sec with 30 sec N_2 flow	
49	Etching 1% HF	Use Beaker HF with 1% ◦ time variable ◦ native oxide strip 1 min or hydrophobic surface Etch rate for: TEOS H3 = 28 nm/min Si3N4 H2 = .33 nm/min	Removal of oxide layer, when oxide is not stripped eutectic bonding will not take place.
50	Quick Dump Rinse (QDR)	QDR: 2 cycles of steps 1 till 3, 1- fill bath 15 sec 2- spray dump 15 sec 3- spray-fill 40 sec 4- end fill 500 sec cascade rinsing: continuous flow Rinse till the DI resistivity is > 10 ΩM	
51	Substrate drying	Single wafer dryer ◦ speed: 2500 rpm, 60 sec with 30 sec N_2 flow	
52	Evaporation of Cr	Balzers BAK600 ◦ Crucible: 3 (Chromium) ◦ Voltage: 8kV ◦ Base pressure: ¡ 1e-6 mBar ◦ Density: 7.2 ◦ Depositionrate: 1 - 20 A/s	50 nm of Cr on the backside of wafer. This layer is needed for measurements in vibrometer
53	Dehydration bake	Dehydration bake on hotplate ◦ temp. 120°C ◦ time: 5min	
54	Priming (liquid)	Primer: HexaMethylDiSilazane (HMDS) use spin coater: ◦ program: 4000 (4000rpm, 30sec)	
55	Coating Olin Oir 907-17	Coating: Primus spinner ◦ olin oir 907-17 ◦ spin Program: 4000 (4000rpm, 30sec) Prebake: hotplate ◦ time 90 sec ◦ temp 95 °C	
56	Alignment & Exposure Olin OiR 907-17	Electronic Vision Group EV620 Mask Aligner ◦ Hg-lamp: 12 mW/cm 2 ◦ Exposure Time: 4sec	

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Table B.1 – *continued from previous page*

Step	Process		Comment
57	Development Olin OiR resist	After exposure Bake : hotplate ∘ time 60sec ∘ temp 120℃ Development: Developer: OPD4262 ∘ time: 30sec in Beaker 1 ∘ time: 15-30sec in Beaker 2	
58	Quick Dump Rinse (QDR)	QDR: 2 cycles of steps 1 till 3, 1- fill bath 15 sec 2- spray dump 15 sec 3- spray-fill 40 sec 4- end fill 500 sec cascade rinsing: continuous flow Rinse till the DI resistivity is $>$ 10 ΩM	
59	Substrate drying	Single wafer dryer ∘ speed: 2500 rpm, 60 sec with 30 sec N_2 flow	
60	Post bake Olin OiR resist	Hotplate ∘ temp 120℃ ∘ time 10min	
61	Inspection by optical microscope	Nikon Microscope ∘ dedicated microscope for lithography inspection	
62	Etching of chromium	Use dedicated Beaker with chromium etch (standard) ∘ temp.:20℃ Etch rates = 60nm/min, Check always the etch rate with dummy wafer.	time: 15 sec
63	Quick Dump Rinse (QDR)	QDR: 2 cycles of steps 1 till 3, 1- fill bath 15 sec 2- spray dump 15 sec 3- spray-fill 40 sec 4- end fill 500 sec cascade rinsing: continuous flow Rinse till the DI resistivity is $>$ 10 ΩM	
64	Etching of gold	∘ Recipe: KI:I2:DI = (4:1:40) ∘ add 40g KI and 10g I_2 to 400ml DI water ∘ temp.: 20℃ Etch rates : check rate with dummy wafer Excessive under etching of Cr occurs because of a galvanic reaction with gold. To minimize this. make sure you do not over etch the chromium.	time: 2 min
65	Quick Dump Rinse (QDR)	QDR: 2 cycles of steps 1 till 3, 1- fill bath 15 sec 2- spray dump 15 sec 3- spray-fill 40 sec 4- end fill 500 sec cascade rinsing: continuous flow Rinse till the DI resistivity is $>$ 10 ΩM	
66	Substrate drying	Single wafer dryer ∘ speed: 2500 rpm, 60 sec with 30 sec N_2 flow	
67	Stripping resist in HNO_3 (99%)	∘ Beaker 0: HNO_3 (99%) ∘ time: $>$ 10 min, depends on the application	
68	Quick Dump Rinse (QDR)	QDR: 2 cycles of steps 1 till 3, 1- fill bath 15 sec 2- spray dump 15 sec 3- spray-fill 40 sec 4- end fill 500 sec cascade rinsing: continuous flow Rinse till the DI resistivity is $>$ 10 ΩM	
69	Substrate drying	Single wafer dryer ∘ speed: 2500 rpm, 60 sec with 30 sec N_2 flow	
70	Inspection by optical microscopic	∘ olympus Microscope (4) and/or ∘ leica Microscope (2)	
71	Dehydration bake	Dehydration bake on hotplate ∘ temp. 120℃ ∘ time: 5min	Prepare some dummy wafers to be used in DRIE step

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Table B.1 – *continued from previous page*

Step	**Process**		**Comment**
72	Priming (liquid)	Primer: HexaMethylDiSilazane (HMDS) use spin coater: ∘ program: 4000 (4000rpm, 30sec)	
73	Coating Olin Oir 907-17	Coating: Primus spinner ∘ olin oir 907-17 ∘ spin Program: 4000 (4000rpm, 30sec) Prebake: hotplate ∘ time 90 sec ∘ temp 95 ℃	
74	Alignment & Exposure Olin OiR 907-17	Electronic Vision Group EV620 Mask Aligner ∘ Hg-lamp: 12 mW/cm 2 ∘ Exposure Time: 4sec	
75	Development Olin OiR resist	After exposure Bake : hotplate ∘ time 60sec ∘ temp 120℃ Development: Developer: OPD4262 ∘ time: 30sec in Beaker 1 ∘ time: 15-30sec in Beaker 2	
76	Quick Dump Rinse (QDR)	QDR: 2 cycles of steps 1 till 3, 1- fill bath 15 sec 2- spray dump 15 sec 3- spray-fill 40 sec 4- end fill 500 sec cascade rinsing: continuous flow Rinse till the DI resistivity is > 10 ΩM	
77	Substrate drying	Single wafer dryer ∘ speed: 2500 rpm, 60 sec with 30 sec N_2 flow	
78	Post bake Olin OiR resist	Post bake: Hotplate ∘ temp 120℃ ∘ time 10min	Time: 20 mins
79	Inspection by optical microscope	Nikon Microscope ∘ dedicated microscope for lithography inspection	
80	DRIE of silicon B- ADIX	Adixen-SE Standard Bosch recipe.	Use dummy wafers to check the process
Parameters	**Etch**	**Deposition**	
Gas	SF6	C4F8	
Flow [sscm]	300	150	
Time [sec]	7	2	
Priority	2	1	
APC %	25	25	
CCP LF [Watt]	80	80	
Pulsed [msec]	10 on/90 off	10 on/90 off	
ICP [watt]	1800	1800	
He [mbar]	10	10	
SH [mm]	200	200	
Eelctrode T℃	10	10	
Er Oir olin (nm/min)	50		
Er silicon (μm/min)	2-10		
81	Inspection by optical microscope	Nikon Microscope	
82	Dehydration bake	Dehydration bake aon hotplate ∘ temp. 120℃ ∘ time: 5min	
83	Priming (liquid))	Primer: HexaMethylDiSilazane (HMDS) use spin coater: ∘ program: 4000 (4000rpm, 30sec)	
84	Lithography Coating Olin OiR 908-35	Coating: Primus coater ∘ Olin OiR 908-35 ∘ Spin Program: 4000 (4000rpm, 30sec) Prebake: Hotplate ∘ Time 120s ∘ temp 95 ℃	
85	Alignment & Exposure Olin 908-35	∘ Electronic Vision Group EV620 Mask Aligner ∘ Hg lamp: 12 mW/cm 2 ∘ Exposure Time: 9sec	

Continued on next page

Table B.1 – *continued from previous page*

Step	Process		Comment
86	Development Olin OiR resist	After exposure Bake : hotplate ∘ time 60sec ∘ temp 120℃ Development: Developer: OPD4262 ∘ time: 30sec in Beaker 1 ∘ time: 15-30sec in Beaker 2	
87	Quick Dump Rinse (QDR)	QDR: 2 cycles of steps 1 till 3, 1- fill bath 15 sec 2- spray dump 15 sec 3- spray-fill 40 sec 4- end fill 500 sec cascade rinsing: continuous flow Rinse till the DI resistivity is > 10 ΩM	
88	Substrate drying	Single wafer dryer ∘ speed: 2500 rpm, 60 sec with 30 sec N_2 flow	
89	Post bake Olin OiR resist	Post bake: Hotplate ∘ temp 120℃ ∘ time 10min	
90	Inspection by Optical microscope	Nikon Microscope ∘ dedicated microscope for lithography inspection	
91	Etching of chromium	Use dedicated Beaker with chromium etch (standard) ∘ temp.:20℃ Etch rates = 60nm/min, Check always the etch rate with dummy wafer.	
92	Quick Dump Rinse (QDR)	QDR: 2 cycles of steps 1 till 3, 1- fill bath 15 sec 2- spray dump 15 sec 3- spray-fill 40 sec 4- end fill 500 sec cascade rinsing: continuous flow Rinse till the DI resistivity is > 10 ΩM	
93	Substrate drying	Single wafer dryer ∘ speed: 2500 rpm, 60 sec with 30 sec N_2 flow	
94	Inspection by Optical microscopic	∘ olympus Microscope (4) and/or ∘ leica Microscope (2)	
95	Dupont MX 5020 foil for DRIE	Material: Dupont MX5020 foil Application: wafer through etching using Adixen SE Procedure: applying MX5020 ∘ Start with the lithography process for etching mask ∘ Remove plastic protection (has no color) from backside of the foil ∘ Apply the foil to the wafer with a roller ∘ Avoid air bubbles, retract the foil if bubbles are present ∘ Protect the photoresist mask with a blue A4 or bare silicon wafer during laminating, ∘ DO NOT use blue tissue, this will get stuck in the laminator ∘ Guide the wafer with foil by hand through the laminator, Temp 90℃, speed 2 ∘ After laminating, the foil will stick to the A4 paper. ∘ Cut around the wafer (leave 1 cm) to separate the A4 paper from the wafer ∘ Remove plastic protection foil carefully ∘ After removing the plastic protection foil, cut-off excess of the blue foil. This should be done accurately, no foil residue should be on the topside of the wafer, otherwise the wafer can get stuck in the Adixen dry etcher.	Front side

Continued on next page

Table B.1 – *continued from previous page*

Step	Process		Comment
		∘ Check if the foil on the outer-edge of the wafer is smooth and does not contain undesired foil residue. This is important to ensure proper helium-backside cooling in the Adxien dry etcher. ∘ Before DRIE etching remove the plastic protection foil!	
		DRIE Adixen: Temperature range: -100℃ up to 20 ℃. Removal of MX5020 ∘ Start with O2 plasma in Tepla 300E (metals are allowed) ∘ Continue with HN03 (99%) ∘ Optional: a piranha solution clean: only when the substrate is metal free!	
96	DRIE of multilayers	Adixen SE Application: directional etch of SiRN or SiO_2	Etching of thermal oxide
	Parameters	**Value**	
	Argon (sccm)	100	
	CHF3 (sccm)	100	
	APC %	100	
	ICP (Watt)	1200	
	CCP (Watt) Rf	150 (Vde=580V)	
	SH (mm)	200	
	Electrode temp.	-100 +20℃	
	He (bar)	10	
	Etch rate Oir resist	160 nm/min	
	Etch rate SiO2	250 nm/min	
	Etch rate silicon	70-80 nm/min	
	Etch rate SU-8	150 nm/min	
	Etchrate SiRN	300 nm/min	
97	DRIE of Si pulsed C4F8 at 40℃	Adixen SE Application: trenches, complete wafer thickness using thick photoresist (908-35) Use: C4F8 flow and CCP for tuning process.	Stop on BOX layer. Use dummy wafers to optimise the profile. Profile should be
Parameters	**Etch**	**Deposition**	negative and oxide
Gas	SF6	C4F8	membrane should be
Flow (sccm)	500	185	free of silicon.
Time (sec)	4	0.5	
Priority	2	1	
APC %	15	15	
ICP (Watt)	2500	2500	
CCP (Watt)	nvt	20	
Pulsed (msec)	nvt	20on/180off	
SH (mm)	110	110	
Electrode temp.	-40℃	-40℃	
He (bar)	10	10	
CCP . . . On/off (w). . . . [msec]	C4F8. . . Er resist (sscm). . . (nm/min)	silicon (μm/min)	
20. . . . 20/180	20. 33-50	10	
20. . . . 35/165	25. 80	10	
98	DRIE of multilayers	Adixen SE Application: directional etch of SiRN or SiO2	Etching of BOX layer (1 um)
	Parameters	**Value**	
	Argon (sccm)	100	
	CHF3 (sccm)	100	
	APC %	100	
	ICP (Watt)	1200	
	CCP (Watt) Rf	150 (Vde=580V)	
	SH (mm)	200	
	Electrode temp.	-100 +20℃	
	He (bar)	10	
	Etch rate Oir resist	160 nm/min	
	Etch rate SiO_2	250 nm/min	

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Table B.1 – *continued from previous page*

Step	Process		Comment
	Etch rate silicon Etch rate SU-8 Etch rate SiRN	70-80 nm/min 150 nm/min 300 nm/min	
99	Clean substrate by drying in air	∘ Beaker IPA VLSI, time 10 min ∘ Substrate drying by air in wet bench	
100	Cleaning piranha	Mixture: H2SO4 :H2O2 (3:1) vol% ∘ start fill; bath is filled H_2SO_4 ∘ continue; the H2O2 is added ∘ temperature will increase till 130℃, set point is 85℃ ∘ cleaning time 15min ∘ Quick Dump Rinse ¡0.1S for spin drying ∘ Quick Dump Rinse short for Semitool Rinse Dryer	
101	Quick Dump Rinse (QDR)	QDR: 2 cycles of steps 1 till 3, 1- fill bath 15 sec 2- spray dump 15 sec 3- spray-fill 40 sec 4- end fill 500 sec cascade rinsing: continuous flow Rinse till the DI resistivity is $>$ 10 ΩM	
102	Clean substrate by drying in air	∘ Beaker IPA VLSI, time 10 min ∘ Substrate drying by air in wet bench	
103	EV620 Aligning & Pre bonding	EV620 mask aligner Program: ∘ SDB Direct Bond tool 4” ∘ Bond chuck SDB ∘ Substrate1 4” ∘ Substrate2 4” ∘ Separation 30 μm ∘ No exposure ∘ SDB Piston ∘ Bond time 60 sec Instructions: ∘ Align align marks of top wafer to crosshairs ∘ Check pre-bonding by using IR-setup	
104			Chip isolation by breaking. See grooves on backside.

Appendix C

Process Parameters (Chapter 7)

Table C.1: Process parameters to fabricate the mechanical element to integrate with the optical waveguide (Chapter 7)

Step	Process		Comment
1	Standard cleaning with 1% HF		
2	LPCVD of SiRN (200-300 Mpa)	Tempress LPCVD G4 Program: ∘ SiH2Cl2 flow: 150sccm ∘ NH3 flow: 50 sccm ∘ temperature: 830/850/870℃ ∘ pressure: 200 mTorr ∘ deposition rate: ± 6,6 nm/min ∘ Nf: ± 2.18 ∘ Stress (range): 200-280 Mpa.	Required thickness : 100 nm
3	Ellipsometer measurement	Plasmos Ellipsometer	Measure the thickness
4	Micro Balance Measurement	Sartortius Micro Balance	Obtain the mass of a bare silicon wafer before depositing poly, and then measure the same wafer after deposition to calculate the absolute thickness of poly
5	LPCVD of Poly Silicon @ 590℃	Program: ∘ SiH4 flow: 50 sccm ∘ temperature: 590℃ ∘ pressure: 250mTorr ∘ deposition rate: 3.4 nm/min ∘ Stress: 30 MPa Maximum thickness: 2.5 um	Required thickness: 50 nm. Time (previous run): 15 mins 20 sec
6	Wet Oxidation of Silicon at 800℃	Check water level of bubbler ∘ Program: ∘ Temp.: 800℃ ∘ Gas: $H_2O + N_2$ (Bubbler)	Time = 5 or 10 mins to get a thin layer of SiO2 to be used as mask for etching polysilicon in TMAH
7	Dehydration bake	Dehydration bake on hotplate ∘ temp. 120℃ ∘ time: 5min	
8	Priming (liquid)	Primer: HexaMethyl DiSilazane (HMDS) use spin coater: ∘ program: 4000 (4000rpm, 30sec)	
9	Coating Olin Oir 907-17	Coating: Primus spinner ∘ olin oir 907-17 ∘ spin Program: 4000 (4000rpm, 30sec) Prebake: hotplate ∘ time 90 sec	

Continued on next page

Table C.1 – *continued from previous page*

Step	Process		Comment
		∘ temp 95 ℃	
10	Alignment & Exposure Olin OiR 907-17	Electronic Vision Group EV620 Mask Aligner ∘ Hg-lamp: 12 mW/cm 2 ∘ Exposure Time: 4sec	
11	Development Olin OiR resist	After exposure Bake : hotplate ∘ time 60sec ∘ temp 120℃ Development: Developer: OPD4262 ∘ time: 30sec in beaker 1 ∘ time: 15-30sec in beaker 2	
12	Quick Dump Rinse (QDR)	QDR: 2 cycles of steps 1 till 3, 1- fill bath 5 sec 2- spray dump 15 sec 3- spray-fill 90 sec 4- end fill 200 sec cascade rinsing: continuous flow Rinse till the DI resistivity is >10.5M	
13	Substrate drying	Single wafer dryer ∘ speed: 2500 rpm, 60 sec with 30 sec N_2 flow	
14	Post bake Olin OiR resist	Post bake: Hotplate ∘ temperature: 120℃ ∘ time 10min	
15	Inspection by optical microscope	Nikon Microscope ∘ dedicated microscope for lithography inspection	
16	Etching in 1% HF multipurpose	Multipurpose use dedicated beaker HF 1% ∘ temperature: 20 ℃. ∘ time: depends on application	etching SiO_2
17	Stripping of resist with acetone	Spray method ∘ start with technical acetone for 100% stripping ∘ time 60sec ∘ finish with VLSI iso-propanol (IPA) ∘ spin drying ∘ visual microscopic inspection	
18	Etching in TMAH (25wt%) standard	Use dedicated beaker : TMAH (25%) standard A HF (1%) dip must have preceded this etching step ∘ temperature: 40℃ ∘ stirrer ∘ Quick Dump Rinse 10.5 MΩ ∘ spin drying	Etch rate (previous run): 16.6 nm/min
Material	**Temp,℃**	**etch rate**	
Poly590	40	60	
ALN	20	22	
19	Etching in HF 50%	Use private beaker : HF 50% standard ∘ temperature: 20℃ Etch rates: ∘ Si_3N_4-H2 = 0.64 nm/min ∘ SiRN-G3# (nanolab) = 3.1 - 3.5 nm/min ∘ SiO2 = 1 m/min	Etch rate: 4 nm/min
20	Wet oxidation of silicon<6 m	Tempress-furnace A3 ∘ Program: ∘ Temp.: 1000,℃ ∘ Gas: O_2 + H_20 injection ∘ Flow: 2+ 4l/min ∘ Ramp: xx℃/min	Thickness required = 2500 nm. Time = 31 hours, oxidation rate: 1.34 nm/min or 80.67 nm/min
21	Ellipsometer measurement	Plasmos Ellipsometer	Measure the layer thickness on a dummy wafer
22	Etching in HF 50%	Use private beaker : HF 50% standard ∘ temperature: 20℃ Etch rates: ∘ Si_3N_4-H_2 = 0.64 nm/min ∘ SiRN-G3# (nanolab) = 3.1 - 3.5 nm/min ∘ SiO2 = 1 μ m/min	Removal of SiN and SiO2
23	Measurement of stress of in thin films	Veeco Dektak 8 Applications: ∘ Stress measurements by	Measure the cavity depth, should be around 1 μm

Continued on next page

Table C.1 – *continued from previous page*

Step	Process		Comment
		scanning wafer curvature ∘ Scan length: 80 mm for a 4" wafer ∘ Stylus force: 5 mg ∘ Duration: 60 sec ∘ Profile: hills and Valleys ∘ Use deflection value at 40 mm for stress calculation	
24	Priming (liquid)	Primer: Hexa Methyl DiSilazane (HMDS) use spin coater: ∘ program: 4000 (4000rpm, 30sec)	Standard cleaning + dehydration bake @ 120 C are required prior to this step
25	Coating Olin Oir 907-17	Coating: Primus spinner ∘ olin oir 907-17 ∘ spin Program: 4000 (4000rpm, 30sec) Prebake: hotplate ∘ time 90 sec ∘ temp 95 ℃	
26	Alignment & Exposure Olin OiR 907-17	Electronic Vision Group EV620 Mask Aligner ∘ Hg-lamp: 12 mW/cm 2 ∘ Exposure Time: 4sec	Mask: Trench
27	Development Olin OiR resist	After exposure Bake : hotplate ∘ time 60sec ∘ temperature: 120℃ Development: Developer: OPD4262 ∘ time: 30sec in beaker 1 ∘ time: 15-30sec in beaker 2	
28	Post bake Olin OiR resist	NL-CLR-WB21 post bake: Hotplate ∘ temp 120℃ ∘ time 10min	Time: 30 mins
29	Lithography Post bake 150 ℃	Heraus Resist Furnace Applications: For Cryogenic DRIE to avoid cracking of resist To fabricate a tapered profile Hotplate 150℃ ∘ Time: 30min	Time: 15 or 30 mins
30	DRIE of Silicon C-CRYO-SF6	Adixen SE program: C.CONT500	Depth needed: 5 μm
	Parameter SF6 [sscm] 02 [sscm] ICP [watt] CCP LF[watt] On/off SH [mm] APC [%] Temp.(℃)	**Value** 100 10-20 500 20 20/180 200 100 -120 - 100	Etch time: 2 mins 5 sec
	Material Silicon [μm/min] Olin oir Si02 (TEOS) SiRN	**etch rate** 2 up to 4 <10 nm/min -	
31	Inspection by optical microscopic	∘ olympus Microscope (4) and/or ∘ leica Microscope (2)	Inspect the profile and etched depth
32	Stripping of resist in oxygen plasma	Tepla300 Barrel Etcher (2.45 GHz) Ultra clean system only (no metals except Al) See list with recipes in CR ∘ O2 flow: 200sccm (50%) ∘ Power: up to 1000W ∘ Pressure: 1 mbar	Time: 1 hour
33	Inspection by optical microscopic	∘ olympus Microscope (4) ∘ leica Microscope (2)	Check the trench width and decide the thickness needed for oxide
34	Wet Oxidation of Silicon @ 1150℃	Furnace B2 ∘ Standby temperature: 800℃ ∘ Check water level of bubbler ∘ Program: WET1150B ∘ Temp.: 1150℃ ∘ Gas: $H_2O + N_2$ (Bubbler)	Requires standard cleaning
35	Ellipsometer	Plasmos Ellipsometer	Measure the thickness

Continued on next page

Table C.1 – *continued from previous page*

Step	Process		Comment
	measurement		with a dummy wafer
36	Micro Balance Measurement	Sartortius Micro Balance	Measure the mass of bare silicon wafer before and after poly deposition to calculate the thickness
37	LPCVD of Poly Silicon @ 590℃	LPCVD F2 Program: ∘ SiH4 flow: 50 sccm ∘ temperature: 590℃ ∘ pressure: 250mTorr ∘ deposition rate: 3.4 nm/min ∘ Stress: 30 MPa Maximum thickness: 2.5 um	Required thickness: 1.5 μ m, Time: 8 hours 5 mins, Deposition rate: 3.09 nm/min
38	Annealing at 1050℃ with N_2	Tempress furnace B3 Standby temperature: 800℃ ∘ Program: ANN1050C ∘ Temp.: 1050℃ ∘ Gas: N_2 ∘ Flow: 1l/min ∘ Ramp: 10℃/min Polysilicon anneal: 60 min	Time = 60 mins
39	LPCVD of SiRN (50-100 Mpa)	LPCVD G3 Program: SiRN01 ∘ SiH2Cl2 flow: 77,5 sccm ∘ NH3 flow: 20 sccm ∘ temperature: 820/850/870℃ ∘ pressure: 150 mTorr ∘ N_2 low: 250 sccm ∘ deposition rate: $\pm$4 nm/min ∘ Nf: $\pm$ 2.18	Standard cleaning and 1%HF cleaning is necessary prior to deposition
40	Sputtering of Cr	-Sputterke Cr Target ∘ Use Ar flow to adjust process pressure. ∘ Base pressure: <1.0 e-6mbar ∘ Sputter pressure: 6.6 e-3mbar ∘ power: 200W ∘ Depositionrate = 15 nm/min	Thickness : 10 nm, Time used : 50 sec+1 min pre-sputtering
41	Sputtering of Au	Sputterke Au Target ∘ Use Ar flow to adjust pressure ∘ Base pressure: <1.0 e-6mbar ∘ Sputter pressure: 6.6 e-3mbar ∘ power: 200W ∘ Deposition rate = 45-50 nm/min. ∘ MAX THICKNESS: 250 NM	Should be done right after Cr deposition, without disturbing the vacuum. Thickness: 100 nm, Time: 2 mins+1 min pre-sputtering
42	Priming (liquid)	Primer: Hexa Methyl DiSilazane (HMDS) use spin coater: ∘ program: 4000 (4000rpm, 30sec)	
43	Coating Olin Oir 907-17	Coating: Primus spinner ∘ olin oir 907-17 ∘ spin Program: 4000 (4000rpm, 30sec) Prebake: hotplate ∘ time 90 sec ∘ temp 95 ℃	
44	Alignment & Exposure Olin OiR 907-17	Electronic Vision Group EV620 Mask Aligner ∘ Hg-lamp: 12 mW/cm 2 ∘ Exposure Time: 4sec	Mask: Metal
45	Development Olin OiR resist	After exposure Bake : hotplate ∘ time 60sec ∘ temp 120℃ Development: Developer: OPD4262 ∘ time: 30sec in beaker 1 ∘ time: 15-30sec in beaker 2	
46	Post bake Olin OiR resist	Post bake: Hotplate ∘ temp 120℃ ∘ time 10min	
47	Etching of gold	Use dedicated beaker with gold etch ∘ Recipe: KI:I2:DI = (4:1:400) ∘ add 40g KI and 10g I2 to 400ml DI water	Etching time: 50 to 60 secs

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Table C.1 – *continued from previous page*

Step	Process		Comment
		∘ Temperature: 20℃ Etch rate = 200 nm/min (check rate with dummy wafer) Excessive under etching of Cr occurs because of a galvanic reaction with gold. To minimize this make sure you do not over etch the Cr.	
48	Etching of chromium	Use dedicated beaker with chromium etch (standard) ∘ temp.:20℃ Etch rate = 60nm/min, Check always the etch rate with dummy wafer.	Etching time: 30 secs
49	Stripping of resist in HNO_3 multipurpose	∘ Beaker : HNO_3 (100%) ∘ time: variable	
50	Dehydration bake	Dehydration bake on hotplate ∘ temp. 120℃ ∘ time: 5min	
51	Priming (liquid)	Primer: Hexa Methyl DiSilazane (HMDS) use spin coater: ∘ program: 4000 (4000rpm, 30sec)	
52	Lithography Coating Olin OiR 908-35	Coating: Primus coater ∘ Olin OiR 908-35 ∘ Spin Program: 4000 (4000rpm, 30sec) Prebake: Hotplate ∘ Time 120s ∘ temp 95 ℃	
53	Alignment & Exposure Olin 908-35	∘ Electronic Vision Group EV620 Mask Aligner ∘ Hg lamp: 12 mW/cm 2 ∘ Exposure Time: 9sec	With mask: SiRN Beams
54	Development Olin OiR resist	After exposure Bake: hotplate ∘ time 60sec ∘ temp 120℃ Development: Developer: OPD4262 ∘ time: 30sec in beaker 1 ∘ time: 15-30sec in beaker 2	
55	Post bake Olin OiR resist	Post bake: Hotplate ∘ temp 120℃ ∘ time 10min	
56	Etching of gold	Use dedicated beaker with gold etch ∘ recipe: KI:I2:DI = (4:1:400) ∘ add 40g KI and 10g I2 to 400ml DI water ∘ temp.: 20℃ Etch rates: 200 nm/min (check rate with dummy wafer) Excessive under etching of Cr occurs because of a galvanic reaction with gold. To minimize this make sure you do not over etch the Cr.	
57	Etching of chromium	Use dedicated beaker with chromium etch (standard) ∘ temp.:20℃ Etch rate: 60nm/min, Check always the etch rate with dummy wafer.	
58	RIE of SiRN	Tetske ∘ Chamber: dirty chamber ∘ Do Not use the Quartz electrode. ∘ Electrode: styros ∘ pressure: 10 mTorr ∘ CHF3 gas flow: 25 sccm ∘ O2 gas flow: 5 sccm ∘ Power: 60 Watt ∘ Vdc: range -500 up to - 540 Volt ∘ Load: 53 ∘ Tune: 36	Thickness to be etched = 1 μ m

Continued on next page

Table C.1 – *continued from previous page*

Step	Process		Comment
		∘ Electrode temp: 10℃	
		Etch rate SiRN: 60 nm/min Etch rate SiO2 (ThOX): 30 nm/min Etch rate Olin resist: 50 nm/min	
59	Stripping of resist in oxygen plasma	Tepla 300E ∘ Barrel Etcher (2.45 GHz) ∘ Multipurpose sytem ∘ O2 flow: 200sccm (50%) ∘ Power: 500W ∘ Pressure: 1.2 mbar Values for olin oir resist: ∘ Time: 10 min for 1-3 wafers, 400 nm/min ∘ Time: 20 min for 4-10 wafers ∘ End point detection by visual inspection of the plasma color. ∘ Blue color means still photoresist on the wafer, purple means clean.	
60	Dehydration bake	Dehydration bake on hotplate ∘ temp. 120℃ ∘ time: 5min	
61	Priming (liquid)	Primer: Hexa Methyl DiSilazane (HMDS) use spin coater: ∘ program: 4000 (4000rpm, 30sec)	
62	Lithography Coating Olin OiR 908-35	Coating: Primus coater ∘ Olin OiR 908-35 ∘ Spin Program: 4000 (4000rpm, 30sec) Prebake: Hotplate ∘ Time 120s ∘ temp 95 ℃	Use 3000 rpm
63	Alignment & Exposure Olin 908-35	∘ Electronic Vision Group EV620 Mask Aligner ∘ Hg lamp: 12 mW/cm 2 ∘ Exposure Time: 9sec	Adjust time with respect to the thickness
64	Development Olin OiR resist	After exposure Bake : hotplate ∘ time 60sec ∘ temperature: 120℃ Development: Developer: OPD4262 ∘ time: 30sec in beaker 1 ∘ time: 15-30sec in beaker 2	
65	Post bake Olin OiR resist	Post bake: Hotplate ∘ temperature: 120℃ ∘ time 10min	
66	Inspection by optical microscope	Nikon Microscope ∘ dedicated microscope for lithography inspection	
67	DRIE of multilayers	Adixen SE Application: directional etch of SiRN or SiO2	To etch 1000 nm Of SiRN
	Parameters	**Value**	
	Argon (sccm)	100	
	CHF3 (sccm)	100	
	APC %	100	
	ICP (Watt)	1200	
	CCP (Watt) Rf	150 (Vde=580V)	
	SH (mm)	200	
	Electrode temp.	-100 +20℃	
	He (bar)	10	
	Etch rate Oir resist	160 nm/min	
	Etch rate SiO_2	250 nm/min	
	Etch rate silicon	70-80 nm/min	
	Etch rate SU-8	150 nm/min	
	Etch rate SiRN	300 nm/min	
68	DRIE of silicon B-ADIX	Adixen-SE Standard bosch recipe.	To etch polysilicon thickness = 1500 nm

Parameters	**Etch**	**Deposition**
Gas	SF6	C4F8

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Table C.1 – *continued from previous page*

Step	Process		Comment
	Flow [sscm]	300	150
	Time [sec]	7	2
	Priority	2	1
	APC %	25	25
	CCP LF [Watt]	80	80
	Pulsed [msec]	10 on/90 off	10 on/90 off
	ICP [watt]	1800	1800
	He [mbar]	10	10
	SH [mm]	200	200
	Electrode T°C	10	10
	Er Oir olin [nm/min]	50	
	Er silicon [μm/min]	2-10	
69	DRIE of multilayers	Adixen SE Application: directional etch of SiRN or SiO_2	Etch SiO2, thickness = 1000 nm
	Parameters	**Value**	
	Argon (sccm)	100	
	CHF3 (sccm)	100	
	APC %	100	
	ICP (Watt)	1200	
	CCP (Watt) Rf	150 (Vde=580V)	
	SH (mm)	200	
	Electrode temp.	-100 +20°C	
	He (bar)	10	
	Etch rate Oir resist	160 nm/min	
	Etch rate SiO_2	250 nm/min	
	Etch rate silicon	70-80 nm/min	
	Etch rate SU-8	150 nm/min	
	Etch rate SiRN	300 nm/min	
70	Plasma etching of Si B-HARS	Adixen AMS 100 SE	
	Parameters	**Etch**	
	Gas	SF6	
	Flow [sscm]	250	
	Time [sec]	3	
	Priority	2	
	APC [%]	100	
	CCP LF [watt]	80	
	Pulsed LF [ms]	10-90	
	ICP [watt]	1500	
	He [mbar]	10	
	SH [mm]	200	
	Eelctrode T[°C]	10	
	Er Oir Olin	25-50 nm/min	
	Er silicon	1-5 μm/min	
71	Stripping of resist in oxygen plasma	Tepla 300E ∘ Barrel Etcher (2.45 GHz) ∘ Multipurpose system ∘ O2 flow: 200sccm (50%) ∘ Power: 500W ∘ Pressure: 1.2 mbar Values for olin oir resist: ∘ Time: 10 min for 1-3 wafers, 400 nm/min ∘ Time: 20 min for 4-10 wafers ∘ End point detection by visual inspection of the plasma color. ∘ Blue color means still photoresist on the wafer, purple means clean.	
72	Lithography AZ 9260	Priming HMDS: WB28 ∘ Furnace: Lab-line Duo-vac-oven ∘ Dehydration bake (150°C, low pressure): 5 min ∘ Vapor prime HMDS at 150 °C: 5 min ∘ Before coating, cool down the wafers to room temperature Coating AZ 9260: WB21 ∘ Spin program: 10 sec @ 300 rpm, 60 sec @ 2400 rpm ∘ Prebake (110°C): 165 sec Exposure: EVG 620 Electronic Vision Group	

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Table C.1 – *continued from previous page*

Step	Process		Comment
		620 Mask Aligner: ∘ Hg-lamp: 12 mW/cm 2 ∘ Exposure mode: interval Exposure: 10 sec Delay: 10 sec Cycle: 3 cycles Development: Developer OPD4262: user made ∘ Time: 7 min ∘ Quick Dump Rinse>10.5 MOhm ∘ Spin drying	
73	Priming (liquid)	Primer: Hexa Methyl DiSilazane (HMDS) use spin coater: ∘ program: 4000 (4000rpm, 30sec)	
74	Coating Olin Oir 907-17	Coating: Primus spinner ∘ olin oir 907-17 ∘ spin Program: 4000 (4000rpm, 30sec) Prebake: hotplate ∘ time 90 sec ∘ temp 95 ℃	
75	Alignment & Exposure Olin OiR 907-17	Electronic Vision Group EV620 Mask Aligner ∘ Hg-lamp: 12 mW/cm 2 ∘ Exposure Time: 4sec	Use blank mask
76	Post bake Olin OiR resist	Post bake: Hotplate ∘ temperature: 120℃ ∘ time 10min	
77	Lithography Post bake 150 ℃	Heraus Resist Furnace Applications: For Cryogenic DRIE to avoid cracking of resist To fabricate a tapered profile Hotplate 150℃ ∘ Time: 30min	
78	Dicing of a Silicon wafer	Disco DAD dicing saw Applications: Silicon wafers, bonded silicon-silicon wafers (max 1.1mm) See #back103 for laminate of Nitto STW T10 dicing foil (80 μ m) See #back104 for laminate of UV dicing foil (250μ m) Parameters dicing: Wafer work size: 110 mm for a standard 100 mm silicon wafer Max. Feed speed: 10 mm/sec X, Y values: correspond respectively to Ch1 and Ch2 and those values are determined by mask layout Saw type: NBC-Z 2050 Select in blade menu: NBC-Z-2050 Blade info: Exposure 1.3 mm (maximum dicing depth for a new blade) Width: 50 μ m Spindle revolutions: 30. 000 rpm Depth settings: Maximum cut depth: 1.1 mm Foil thickness: See foil info Min. blade height: 50 μ m	
79	Development Olin OiR resist	After exposure Bake : hotplate ∘ time 60sec ∘ temp 120℃ Development: Developer: OPD4262 ∘ time: 30sec in beaker 1 ∘ time: 15-30sec in beaker 2	
80	XeF_2 SLE of polysilicon590	Xactive etcher Always apply a pretreatment step to avoid extreme delay effects.	
	Pressure . . .Delay	**Etch rate . . . CycleT**	

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Table C.1 – *continued from previous page*

Step	Process	Comment
	[Torr] . . . **[cycles]** 2 . . . . . 1.6 3 . . . . . 1.4 4 . . . . . 1.0	**[um/cylce]**. . . **[sec]** 2.2 . . . . . 30 4.9 . . . . . 30 6.2 30	
81	Stripping of resist in oxygen plasma	Tepla 300E ∘ Barrel Etcher (2.45 GHz) ∘ Multipurpose system ∘ O2 flow: 200sccm (50%) ∘ Power: 500W ∘ Pressure: 1.2 mbar Values for olin oir resist: ∘ Time: 10 min for 1-3 wafers, 400 nm/min ∘ Time: 20 min for 4-10 wafers ∘ End point detection by visual inspection of the plasma color. ∘ Blue color means still photoresist on the wafer, purple means clean.

Appendix D

Process Parameters (Chapter 7)

Table D.1: Process parameters to fabricate A-shape TripleX waveguide to be integrated with the mechanical chip (Chapter 7)

Step	Process		Comment
1	Clean HNO3-1	Beaker 1: HNO_3 (99%) 5min	Use Si wafer with 8 μm or 6 μm oxide
2	Clean HN03-2	Beaker 2 : HNO_3 (99%) 5min	
3	Quick Dump Rinse (QDR)	QDR: 2 cycles of steps 1 till 3, 1- fill bath 5 sec 2- spray dump 15 sec 3- spray-fill 90 sec 4- end fill 200 sec cascade rinsing: continuous flow Rinse till the DI resistivity is ¿ 10.5MΩ	
4	Clean HNO_3-3a/b	Beaker 3a/b: HNO_3 (69%), ∘ temperature: 95°C, ∘ time ¿ 10min	
5	Quick Dump Rinse (QDR)	QDR: 2 cycles of steps 1 till 3, 1- fill bath 5 sec 2- spray dump 15 sec 3- spray-fill 90 sec 4- end fill 200 sec cascade rinsing: continuous flow Rinse till the DI resistivity is ¿ 10.5MΩ	
6	Etching in HF 1% (metal free)	Use beaker HF 1% ∘ time variable ∘ native oxide strip: ¿ 1 min or hydrophobic surface etch rate: TEOS H3 (new): 28 nm/min Si_3N_4 H_2 (new): 0.33 nm/min	
7	Quick Dump Rinse (QDR)	QDR: 2 cycles of steps 1 till 3, 1- fill bath 5 sec 2- spray dump 15 sec 3- spray-fill 90 sec 4- end fill 200 sec cascade rinsing:	

Continued on next page

Table D.1 – *continued from previous page*

Step	Process		Comment
		continuous flow Rinse till the DI resistivity is ¿ 10.5MΩ	
8	Substrate drying	Single wafer dryer ∘ speed: 2500 rpm, 60 sec with 30 sec N2 flow	
9	Substrate rinsing/drying Semitool	Semitool spin rinse dryer Use dedicated wafer carrier of rinse dryer Parameters/step ∘ rinse in DI: 30 sec: 600 rpm ∘ rinse in DI: 12.0 M; 600 rpm ∘ N2 purge: 30sec; 600 rpm ∘ drying 1: 150 sec; 1600 rpm ∘ drying 2: 0000 - 0000 Unload wafers	
10	LPCVD of Si_3N_4	LPCVD H_2 ∘ Program: N2 ∘ SiH_2Cl2 flow: 50 sccm ∘ NH_3 flow: 150 sccm ∘ temperature: 800℃ ∘ pressure: 250 mTorr ∘ Stress: 880 ± 30 MPa ∘ deposition rate: 4.74nm/min (200 nm) ∘ deposition rate: 4.34 nm/min (50 nm) ∘ wafer non-uniformity: 0.9 % ∘ boat non-uniformity: 0.3 % ∘ Nf: 2.030	Required Thickness: 150 nm, Deposition rate: 4.308 nm/min Time needed: 34:49 mins
11	LPCVD of SiO_2 (TEOS)	LPCVD H3 ∘ Program: N2 ∘ TEOS flow: 40 sccm ∘ Bubbler N2 : 30 sccm ∘ temperature: 710 C (Z1), 725C (Z2), 740℃ (Z3) ∘ pressure: 400 mTorr ∘ Stress: 282 ± 13 MPa (after anneal @1150℃, 3hr) ∘ deposition rate: 8.1 nm/min (1100 nm) ∘ wafer non-uniformity: 3.6 % ∘ boat non-uniformity: 1.0 % ∘ Nf: 1.434	Thickness: 1100 nm, Deposition rate: 8.1 nm/min Time: 2 hours 16 mins
12	Annealing at 1150 C for 3 hours		
13	Clean HNO_3-1	Beaker 1: HNO_3 (99%) 5min	
14	Clean HN03-2	Beaker 2 : HNO_3 (99%) 5min	
15	Quick Dump Rinse (QDR)	QDR: 2 cycles of steps 1 till 3, 1- fill bath 5 sec 2- spray dump 15 sec 3- spray-fill 90 sec 4- end fill 200 sec cascade rinsing: continuous flow Rinse till the DI resistivity is ¿ 10.5MΩ	
16	Clean HNO_3-3a/b	Beaker 3a/b: HNO_3 (69%), ∘ temp 95℃,	

Continued on next page

Table D.1 – *continued from previous page*

Step	Process		Comment
		∘ time ¿ 10min	
17	Quick Dump Rinse (QDR)	QDR: 2 cycles of steps 1 till 3, 1- fill bath 5 sec 2- spray dump 15 sec 3- spray-fill 90 sec 4- end fill 200 sec cascade rinsing: continuous flow Rinse till the DI resistivity is ¿ 10.5MΩ	
18	Substrate drying	Single wafer dryer ∘ speed: 2500 rpm, 60 sec with 30 sec N2 flow	
19	Substrate rinsing/drying Semitool	Semitool spin rinse dryer Use dedicated wafer carrier of rinse dryer Parameters/step ∘ rinse in DI: 30 sec: 600 rpm ∘ rinse in DI: 12.0 MΩ; 600 rpm ∘ N2 purge: 30sec; 600 rpm ∘ drying 1: 150 sec; 1600 rpm ∘ drying 2: 0000 - 0000 Unload wafers	
20	Dehydration bake	Dehydration bake on hotplate ∘ temp. 120℃ ∘ time: 5min	
21	Priming (liquid)	Primer: Hexa Methyl DiSilazane (HMDS) use spin coater: ∘ program: 4000 (4000rpm, 30sec)	
22	Coating Olin Oir 907-17	Coating: Primus spinner ∘ olin oir 907-17 ∘ spin Program: 4000 (4000rpm, 30sec) Prebake: hotplate ∘ time 90 sec ∘ temp 95℃	
23	Alignment & Exposure Olin OiR 907-17	Electronic Vision Group EV620 Mask Aligner ∘ Hg-lamp: 12 mW/cm^2 ∘ Exposure Time: 4sec	Mask : Inner core (M1)
24	Development Olin OiR resist	After exposure Bake on hotplate ∘ time 60sec ∘ temp 120℃ Development: Developer: OPD4262 ∘ time: 30sec in beaker 1 ∘ time: 15-30sec in beaker 2	
25	Quick Dump Rinse (QDR)	QDR: 2 cycles of steps 1 till 3, 1- fill bath 5 sec 2- spray dump 15 sec 3- spray-fill 90 sec 4- end fill 200 sec cascade rinsing: continuous flow Rinse till the DI resistivity is $>$ 10.5MΩ	
26	Substrate drying	Single wafer dryer ∘ speed: 2500 rpm, 60 sec with 30 sec N_2 flow	
27	Post bake Olin OiR resist	Post bake: Hotplate ∘ temp 120℃ ∘ time 10min	
28	Inspection by optical microscope	Nikon Microscope ∘ dedicated microscope	

Continued on next page

Table D.1 – *continued from previous page*

Step	Process		Comment
		for lithography inspection	
29	Plasma etching of SiN, SiO_2, Si	Plasmatherm 790 Program: Etch0 ∘ Aluminum electrode ∘ Electrode temp.: 20°C ∘ CHF3: 27 sccm ∘ 02: 3 sccm ∘ pressure: 20 mTorr ∘ Power: 350 Watt Silicon: 10 nm/min SiO_2: 34 nm/min SiN: 34 nm/min	Etching both TEOS and Si_3N_4
30	Stripping of resist in oxygen plasma	Tepla300 Barrel Etcher (2.45 GHz) Ultra clean system only (no metals except Al) See list with recipes in CR ∘ O2 flow: 200sccm (50%) ∘ Power: up to 1000W ∘ Pressure: 1 mbar	
31	Clean HNO_3-1	Beaker 1: HNO_3 (99%) 5min	
32	Clean HN03-2	Beaker 2 : HNO_3 (99%) 5min	
33	Quick Dump Rinse (QDR)	QDR: 2 cycles of steps 1 till 3, 1- fill bath 5 sec 2- spray dump 15 sec 3- spray-fill 90 sec 4- end fill 200 sec cascade rinsing: continuous flow Rinse till the DI resistivity is $>$ 10.5MΩ	
34	Clean HNO_3-3a/b	Beaker 3a/b: HNO_3 (69%), ∘ temp 95°C, ∘ time $>$ 10min	
35	Quick Dump Rinse (QDR)	QDR: 2 cycles of steps 1 till 3, 1- fill bath 5 sec 2- spray dump 15 sec 3- spray-fill 90 sec 4- end fill 200 sec cascade rinsing: continuous flow Rinse till the DI resistivity is $>$ 10.5MΩ	
36	Substrate drying	Single wafer dryer ∘ speed: 2500 rpm, 60 sec with 30 sec N2 flow	
37	Substrate rinsing/drying Semitool	NL-CLR-Wet Benches Semitool spin rinse dryer Use dedicated wafer carrier of rinse dryer Parameters/step ∘ rinse in DI: 30 sec: 600 rpm ∘ rinse in DI: 12.0 ΩM; 600 rpm ∘ N2 purge: 30sec; 600 rpm ∘ drying 1: 150 sec; 1600 rpm ∘ drying 2: 0000 - 0000 Unload wafers	
38	LPCVD of Si_3N_4	LPCVD H_2 ∘ Program: N2 ∘ SiH_2Cl_2 flow: 50 sccm	Thickness: 150 nm

Continued on next page

Table D.1 – *continued from previous page*

Step	Process		Comment
		∘ NH_3 flow: 150 sccm ∘ temperature: 800 ℃ ∘ pressure: 250 mTorr ∘ Stress: 880 ± 30 MPa ∘ deposition rate: 4.74nm/min (200 nm) ∘ deposition rate: 4.34 nm/min (50 nm) ∘ wafer non-uniformity: 0.9 % ∘ boat non-uniformity: 0.3 % ∘ Nf: 2.030	
39	LPCVD of SiO_2 (TEOS)	LPCVD H3 ∘ Program: N_2 ∘ TEOS flow: 40 sccm ∘ Bubbler N2 : 30 sccm ∘ temperature: 710 ℃ (Z1), 725℃ (Z2), 740℃ (Z3) ∘ pressure: 400 mTorr ∘ Stress: 282 ± 13 MPa (after anneal @1150℃, 3hr) ∘ deposition rate: 8.1 nm/min (1100 nm) ∘ wafer non-uniformity: 3.6 % ∘ boat non-uniformity: 1.0 % ∘ Nf: 1.434	Thickness: 1100 nm
40	Annealing at 1150℃ for 3 hours		
41	PECVD of SiO_2	OXFORD Plasmalab 80 + Multi-user system Apply purge sequence before and after use Purge sequence: 1 min N_2, pump down, apply three times Parameters: ∘ Electrode temp.: 300℃ ∘ 2% SiH_4/N_2 flow: 200sccm ∘ N_2O flow: 710sccm ∘ pressure: 650mTorr ∘ APC: 33 ∘ power: 60W LF ∘ Capacitor: 850 ∘ Deposition rate: 30 nm/min	Required Thickness: 4 μm
42	Annealing at 1150 C for 3 hours		
43	Chemical mechanical polishing (CMP)		
44	Clean HNO_3-1	Beaker 1: HNO_3 (99%) 5min	
45	Clean HN03-2	Beaker 2 : HNO_3 (99%) 5min	
46	Quick Dump Rinse (QDR)	QDR: 2 cycles of steps 1 till 3, 1- fill bath 5 sec 2- spray dump 15 sec 3- spray-fill 90 sec 4- end fill 200 sec cascade rinsing: continuous flow Rinse till the DI resistivity is $> 10.5M\Omega$	
47	Clean HNO_3-3a/b	Beaker 3a/b:	

Continued on next page

Table D.1 – *continued from previous page*

Step	Process		Comment
		HNO_3 (69%), ∘ temp 95℃, ∘ time > 10min	
48	Quick Dump Rinse (QDR)	QDR: 2 cycles of steps 1 till 3, 1- fill bath 5 sec 2- spray dump 15 sec 3- spray-fill 90 sec 4- end fill 200 sec cascade rinsing: continuous flow Rinse till the DI resistivity is > 10.5ΩM	
49	Substrate drying	Single wafer dryer ∘ speed: 2500 rpm, 60 sec with 30 sec N_2 flow	
50	Substrate rinsing/drying Semitool	Semitool spin rinse dryer Use dedicated wafer carrier of rinse dryer Parameters/step ∘ rinse in DI: 30 sec: 600 rpm ∘ rinse in DI: 12.0 MΩ; 600 rpm ∘ N2 purge: 30sec; 600 rpm ∘ drying 1: 150 sec; 1600 rpm ∘ drying 2: 0000 - 0000 Unload wafers	
51	Dehydration bake	Dehydration bake on hotplate ∘ temp. 120℃ ∘ time: 5min	
52	Priming (liquid)	Primer: Hexa Methyl DiSilazane (HMDS) use spin coater: ∘ program: 4000 (4000rpm, 30sec)	
53	Coating Olin Oir 907-17	Coating: Primus spinner ∘ Olin Oir 907-17 ∘ spin Program: 4000 (4000rpm, 30sec) Prebake: hotplate ∘ time 90 sec ∘ temp 95℃	
54	Alignment & Exposure Olin OiR 907-17	Electronic Vision Group EV620 Mask Aligner ∘ Hg-lamp: 12 mW/cm^2 ∘ Exposure Time: 4sec	Mask : Top cladding etch (M2)
55	Development Olin OiR resist	After exposure Bake : hotplate ∘ time 60sec ∘ temp 120℃ Development: Developer: OPD4262 ∘ time: 30sec in beaker 1 ∘ time: 15-30sec in beaker 2	
56	Quick Dump Rinse (QDR)	QDR: 2 cycles of steps 1 till 3, 1- fill bath 5 sec 2- spray dump 15 sec 3- spray-fill 90 sec 4- end fill 200 sec cascade rinsing: continuous flow Rinse till the DI resistivity is > 10.5MΩ	
57	Substrate drying	Single wafer dryer ∘ speed: 2500 rpm, 60 sec with 30 sec N_2 flow	
58	Post bake Olin OiR resist	Post bake: Hotplate ∘ temp 120℃ ∘ time 10min	

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Table D.1 – *continued from previous page*

Step	Process		Comment
59	Inspection by optical microscope	Nikon Microscope ∘ dedicated microscope for lithography inspection	
60	DRIE of SiO_2	Adixen AMS 100 DE Application: < 5 μm etch depth	Thickness to be Etched: 4.8 or 4.9 μm
	Parameters	**Value**	
	C_4F_8 [sccm]	15	
	He [sccm]	150	
	CH_4 [sccm]	15	
	He-backside cooling	10	
	ICP [watt]	2800	
	CCP [Watt]	350	
	p [mbar]	8.5 x10^{-3}	
	Electrode temp.[°C]	-10	
	Substrate height [mm]	120	
	Etch rate SiO_2 [μm/min]	0.470-0.530	
	Etch rate Olin 907 [nm/min]	ca. 50	
	Etchrate α-Si (nm/min)	-	
	Etch rate SiRN [μm/min]	ca. 30- 100- variable	
61	Etching SiO_2 BHF (1:7)	Use private beaker with BHF (1:7) ∘ temp.: 20°C Etch rates: ∘ thermal SiO_2: 60-80nm/min ∘ PECVD $Si0_2$: 125/nm/min ∘ TEOS SiO_2: 180/nm/min ∘ TEOS H3 (new): 242 nm/min ∘ Pyrex #7740: 20nm/min ∘ Borofloat BF33: 20-25 nm/min ∘ $Si_3N_4 - H_2$: 0.64 nm/min	Etch till seeing the etch stop markings: smiley and cross structures
62	Surface profile measurement	Veeco Dektak 8	Measure and inspect on the cross structures
63	Stripping resist in HNO_3 (99%) multipurpose	Beaker : HNO_3 (99%) ∘ time: $>$ 10 min, depends on the application	
64	Clean HNO_3-1	Beaker 1: HNO_3 (99%) 5min	
65	Clean HN03-2	Beaker 2 : HNO_3 (99%) 5min	
66	Quick Dump Rinse (QDR)	QDR: 2 cycles of steps 1 till 3, 1- fill bath 5 sec 2- spray dump 15 sec 3- spray-fill 90 sec 4- end fill 200 sec cascade rinsing: continuous flow Rinse till the DI resistivity is $>$ 10.5MΩ	
67	Clean HNO_3-3a/b	Beaker 3a/b: HNO_3 (69%), ∘ temp 95°C, ∘ time $>$ 10min	
68	Quick Dump Rinse (QDR)	QDR: 2 cycles of steps 1 till 3, 1- fill bath 5 sec 2- spray dump 15 sec 3- spray-fill 90 sec 4- end fill 200 sec cascade rinsing: continuous flow Rinse till the DI resistivity is	

Continued on next page

Table D.1 – *continued from previous page*

Step	Process		Comment
		$>$ 10.5MΩ	
69	Substrate drying	Single wafer dryer ∘ speed: 2500 rpm, 60 sec with 30 sec N_2 flow	
70	Substrate rinsing/drying Semitool	NL-CLR-Wet Benches Semitool spin rinse dryer Use dedicated wafer carrier of rinse dryer Parameters/step ∘ rinse in DI: 30 sec: 600 rpm ∘ rinse in DI: 12.0 MΩ; 600 rpm ∘ N_2 purge: 30sec; 600 rpm ∘ drying 1: 150 sec; 1600 rpm ∘ drying 2: 0000 - 0000 Unload wafers	
71	Dehydration bake	Dehydration bake on hotplate ∘ temp. 120℃ ∘ time: 5min	
72	Priming (liquid)	Primer: Hexa Methyl DiSilazane (HMDS) use spin coater: ∘ program: 4000 (4000rpm, 30sec)	
73	Coating Olin Oir 907-17	Coating: Primus spinner ∘ olin oir 907-17 ∘ spin Program: 4000 (4000rpm, 30sec) Prebake: hotplate ∘ time 90 sec ∘ temp 95 ℃	
74	Alignment & Exposure Olin OiR 907-17	Electronic Vision Group EV620 Mask Aligner ∘ Hg-lamp: 12 mW/cm^2 ∘ Exposure Time: 4sec	
75	Development Olin OiR resist	After exposure Bake : hotplate ∘ time 60sec ∘ temp 120℃ Development: developer: OPD4262 ∘ time: 30sec in beaker 1 ∘ time: 15-30sec in beaker 2	
76	Quick Dump Rinse (QDR)	QDR: 2 cycles of steps 1 till 3, 1- fill bath 5 sec 2- spray dump 15 sec 3- spray-fill 90 sec 4- end fill 200 sec cascade rinsing: continuous flow Rinse till the DI resistivity is $>$ 10.5MΩ	
77	Substrate drying	Single wafer dryer ∘ speed: 2500 rpm, 60 sec with 30 sec N_2 flow	
78	Inspection by optical microscope	Nikon Microscope ∘ dedicated microscope for lithography inspection	
79	Etching SiO_2 BHF (1:7)	Use private beaker with BHF (1:7) ∘ temp.: 20℃ Etch rates: ∘ thermal SiO_2: 60-80nm/min ∘ PECVD Si02: 125/nm/min ∘ TEOS SiO_2:	Etch depth: 100 nm

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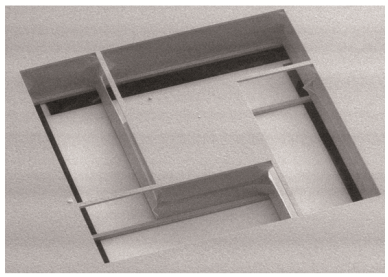
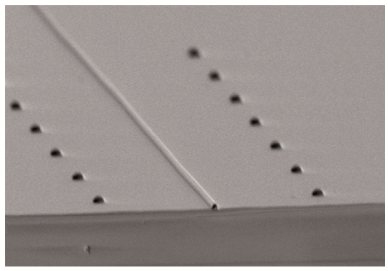
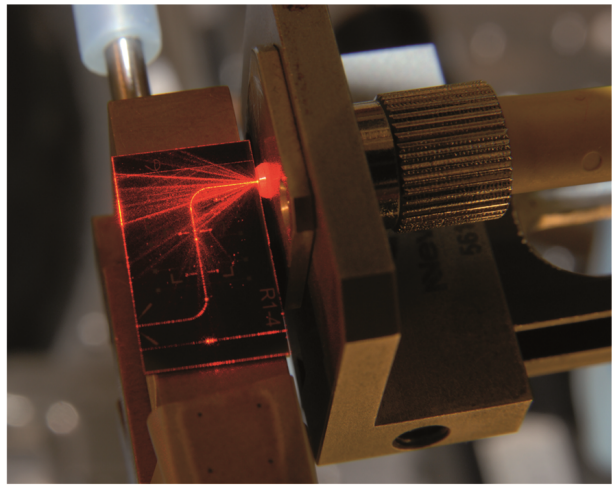
Table D.1 – *continued from previous page*

Step	Process		Comment
		180/nm/min ∘ TEOS H3 (new): 242 nm/min ∘ Pyrex #7740: 20nm/min ∘ Borofloat BF33: 20-25 nm/min ∘ Si_3N_4-H_2: 0.64 nm/min	
80	Evaporation of Cr	Balzers BAK600 ∘ Crucible: 3 (Chromium) ∘ Voltage: 8kV ∘ Emission current: see mis logbook ∘ Base pressure: < 1e-6 mBar ∘ Density: 7.2 ∘ Deposition rate: 1 - 20 A/s	Thickness:10 nm (adhesion layer)
81	Evaporation of Au	Balzers BAK 600 ∘ Crucible: 2 (Au) ∘ Voltage: 10 kV ∘ Emission Current: see mis logbook ∘ Base pressure: < 1e-6 mBar ∘ Density 19.3 g/cm3 ∘ Deposition rate 1-10 A/s Max. thickness: 500nm	Thickness: 100 nm
82	Liftoff	10 mins in acetone, 10 mins in IPA (VLSI)	
83	Dicing of a Silicon wafer	Disco DAD dicing saw Applications: Silicon wafers, bonded silicon-silicon wafers (max 1.1mm) See #back103 for laminate of Nitto STW T10 dicing foil (80 μm) See #back104 for laminate of UV dicing foil (250μm) Parameters dicing: Wafer work size: 110 mm for a standard 100 mm silicon wafer Max. Feed speed: 10 mm/sec X, Y values: correspond respectively to Ch1 and CH_2 and those values are determined by mask layout Saw type NBC-Z 2050 Select in blade menu: NBC-Z-2050 Blade info: Exposure 1.3 mm (maximum dicing depth for a new blade) Width: 50 μm Spindle revolutions: 30. 000 rpm Depth settings: Maximum cut depth: 1.1 mm Foil thickness: See foil info Min. blade height: 50 μm	







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